EC Grant Agreement n°609788

CHEETAH

Cost-reduction through material optimisation and Higher EnErgy outpuT of solAr pHotovoltaic modules - joining Europe's Research and Development efforts in support of its PV industry

Deliverable

D8.20 – Interconnected thin-film modules with 12% conversion efficiency using cost-effective and scalable processes

WP8 – Module development for ultrathin x-Si cells and thin-films

Section 1 – Document Status

Document information

Deliverable name	Interconnected thin-film modules with 12% conversion efficiency using cost-effective and scalable processes
Lead beneficiary	EPFL
Due delivery date from Annex I	M48
Actual / forecast delivery date	M48
Dissemination level	Restricted

Document validation

Name	Organisation	Date	Visa
Paul. M. Sommeling –WP8 leader	ECN	13.12.2017	OK
Jan Kroon - Coordinator	ECN	18.12.2017	OK

Document history

Version	Date	Modifications	Name
V0	12.12.2017	1st draft version submitted to WP8 coordinator	N. Wyrsch
V1	13.12.2017	comments	P.M. Sommeling/ Jan Kroon
V2	13.12.2017	comments	Karsten Bittkau
VF	18.12.2017	Final version approved by coordinator	Jan Kroon

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Section 3 – Executive summary

Description of the deliverable content and purpose

The present deliverable report is related to work performed in task 8.7 for the development of an interconnection scheme for liquid phase crystalized (LPC) Si modules. The goal was to demonstrate mini-modules (with interconnected cells) with an efficiency value > 12% fabricated using a cost effective and scalable process. Thin-film solar cells offer the benefit of monolithic interconnection of cells deposited on the same substrates to form fully integrated modules. Such a connection scheme is well mastered for state-of-the-art industrial thin film modules. In case of LPC-Si, a monolithic interconnection scheme has been developed by HZB in a similar fashion as the one used in production by CSG Solar (Germany) for solid phase crystallized (SPC) Si. This work was reported in the deliverable report D8.17 and is briefly summarized in this report. While it is a proven scalable process, more cost-effective alternatives are desired. We here report on a possible scalable and cost effective solution for the interconnection of LPC-Si cells developed by EPFL. For the latter, we introduced an innovative tunneling contact scheme originally developed for back contacted c-Si cells. We also report on the development by Jülich of direct laser lithography as a scalable process for contact patterning for LPC Si cells and modules.

Brief description of the state of the art and the innovation brought

LPC Silicon on glass cells require a specific interconnection scheme. Up to now, it was derived from the interconnection scheme developed by the company CSG for recrystallized Si on glass. The process involves wet chemistry and laser scribing to create point contacts which are later connected by interdigitated metal lines. Despite validation of the concept, the process is rather complicated and more cost effective solutions are desired.

The alternative interconnection with tunneling contacts proposed here also involves laser scribing, ink-jet printing and wet chemistry. However, it enables a simplification of the interconnection process and should be more cost effective. The results are still far from the defined target efficiency of 12 % but the analysis shows a potential how to achieve it. This work also validates the use of tunneling contacts for LPC-Si cells. As an alternative scalable method, direct laser patterning is also demonstrated.

Section 4 – Deliverable report

1. Introduction

LPC-Si, is a large-grained Si material typically 10 – 20 µm thick and considered as an alternative to (thin) crystalline silicon wafers (typically 100 – 180 µm thick). It has been extensively investigated at HZB in the past years and with the absorber material development, cell efficiencies of more than 15% [1] have been achieved for small cells. However, cell efficiencies are still limited by an insufficient contacting. Different from wafers, with both sides accessible for contacting, for LPC-Si only one side of the absorber can be contacted. Therefore, this technology requires a backside-contacting (BC) scheme with both contact polarities (absorber- and emitter contact) on the same side. This has the advantage of avoiding optical shading by the metal contacts at the front, but in order to utilize this advantage it is important to minimize losses due to "electrical shading" at the back side. This refers to the fact that minority carriers generated below the absorber contact need to traverse laterally to the emitter region. For the LPC-Si absorber, the minority diffusion length is only about 10 – 20 µm and therefore in order to avoid electrical shading, the absorber contact dimension (width) would need to be in that range (and the contacts would have to be passivated). As reported in a previous deliverable report (D8.17), a working strategy is to minimize electrical shading with the use of point contacts which cover only a very small part of the cell area and therefore limit the loss to a very small percentage. Secondly, due to the small absorber thickness and, hence high sheet resistance, the optimum distance between absorber contacts (pitch) is smaller than typically used for c-Si wafer cells. Another challenge is to realize low contact resistances, which becomes even more important for BC cells, since the total contact area is smaller than a double-side contacted solar cell. Due to the specific properties of LPC-Si, i.e. high sheet resistance and small diffusion length, point contacts are suggested to be the ideal BC concept, due to the minimal absorber contact area.

The present deliverable reports on an interconnection scheme that enables a simplification of the fabrication process (with respect to the state-of-the-art scheme reported earlier and summarized here) and achieving low contact resistance thanks to a tunneling contact concept.

1 P. Sonntag et al, "Silicon Solar Cells on Glass with Power Conversion Efficiency above 13% at Thickness below 15 Micrometer , Scientific Reports 7 (2017) 873, DOI:10.1038/s41598-017-00988-x

2. Interconnection scheme for LPC Si on glass modules

2.1. Background

In 1991, the Australian company Pacific Solar (UNSW based) patented a point-contact scheme for contacting and monolithically interconnecting solid phase crystallized (SPC) silicon based solar cells on glass using a resin as the insulating and structuring layer. After much development this resulted in an efficiency of 10.4% for a fully series connected solar cell [2] and was scaled up for production by CSG Solar (Germany). For SPC silicon the initial doping profile is maintained during crystallization and it was thus possible to create thin, highly doped regions in the crystalline silicon layers. These could be used as front side emitter and back surface field and could be contacted with a metal yielding low contact resistances. However, using liquid phase crystallized silicon, a uniformly doped Si layer is obtained, which is too lowly doped for direct contacting with metal. Therefore, the CSG contacting scheme had to be adapted to fit the requirements of liquid phase crystallized silicon.

2.2. "CSG-type" contacting scheme

In contrast to the UNSW group using n/p homo-junction [3], HZB decided to use the a-Si/c-Si heterojunction concept, using thin amorphous silicon layers for passivating and contacting the surface plus a TCO contacting layer (schematically shown in Figure 1a). After depositing these layers, an isolation scribe which defines the cell area, is created with an IR picosecond (ps) laser from the glass side. Subsequently an organic white resin (P150W) layer is applied by spin coating. Then the resin is opened for the absorber contact either by KOH etching with an inkjet printer, as done by CSG, or by laser ablation as described in [4]. The result can be seen in Figure 1b and e. This is followed by the TCO and the emitter wet etch which expose the absorber point contacts. In order to prevent shunting between the TCO and the absorber contact, the sample is then placed in a solvent atmosphere where the resin re-flows back several µm and covers the TCO in a self-aligned manner. Subsequently, the resin is opened for the emitter point contacts using again the inkjet or a laser process similar to the absorber contacts (Figure 1c). Ag is finally deposited on top.

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[2] M. Keevers, T.L. Young, U. Schubert, and M.A. Green, "10% Efficient CSG minimodules," in Proceedings of the 22nd EUPVSEC, 2007, p. p. 1783

[3]J. Dore, D. Ong, S. Varlamov, R. Egan, and M. A. Green, "Progress in Laser-Crystallized Thin-Film Polycrystalline Silicon Solar Cells: Intermediate Layers, Light Trapping, and Metallization," IEEE J. Photovolt., vol. 4, no. 1, pp. 33–39, Jan. 2014

[4] M. Weizman, H. Rhein, J. Dore, S. Gall, C. Klimm, G. Andrä, C. Schultz, F. Fink, B. Rau, and R. Schlatmann, "Efficiency and stability enhancement of laser-crystallized polycrystalline silicon thin-film solar cells by laser firing of the absorber contacts," Sol. Energy Mater. Sol. Cells, vol. 120, Part B, pp. 521–525, Jan. 2014.

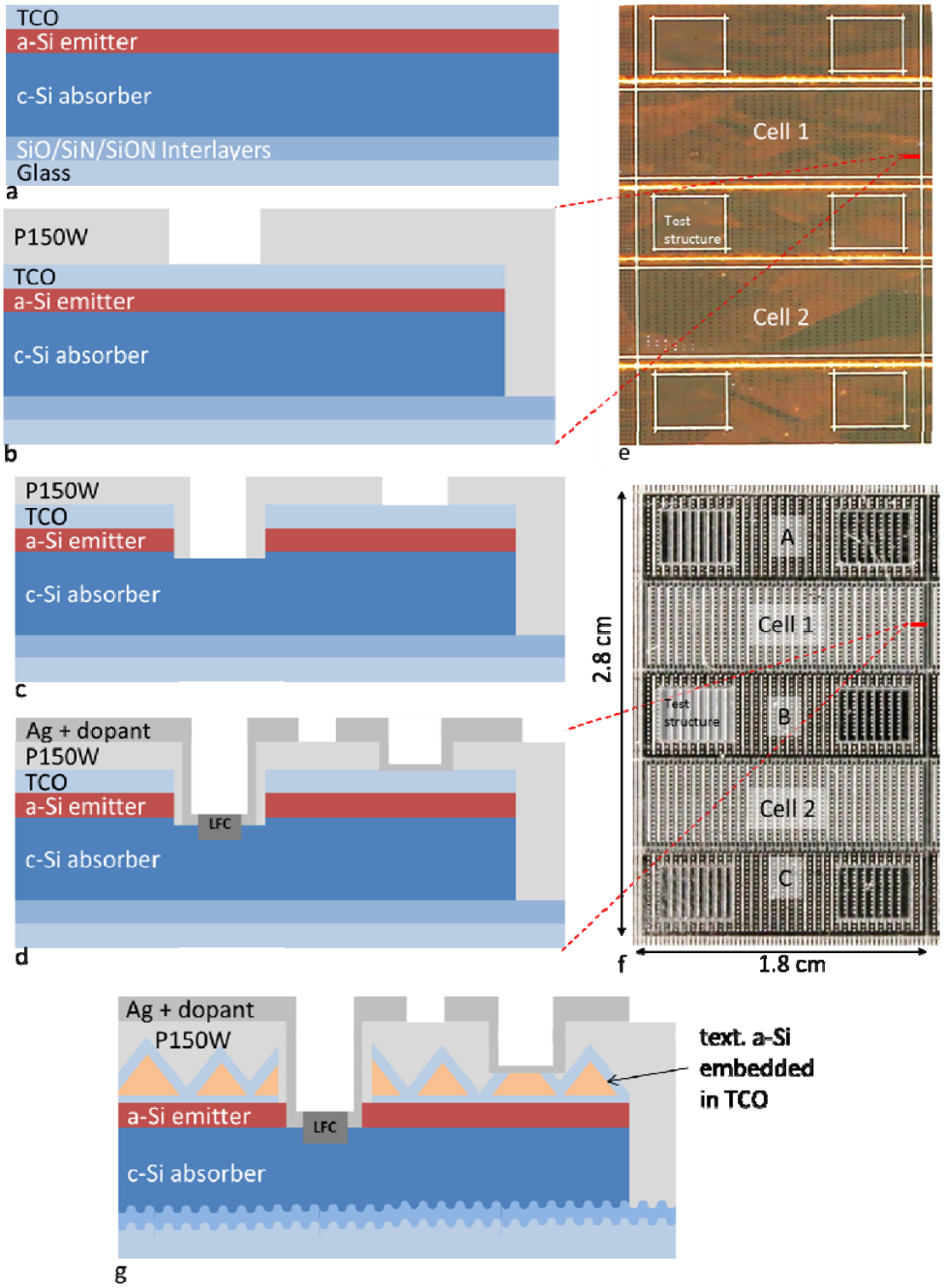


Figure 1: *Schematic cross-section description of the point contact process (a-d) and corresponding top-view images of the sample (e-f). For image e the light is coming from the glass side. The red lines show how the cross sections fit into the sample. The imprinted glass texture and the textured back surface for improved light management from WP9 will be compatible with the contacting and interconnection scheme (g). The textured a-Si layer will be embedded into the TCO layer.*

The Ag provides optimum reflection and a good contact to the TCO. Additional point-contact laser-firing has been developed for a low absorber point-contact resistance [5]. Finally the metal is patterned with a UV ps laser from the back (metal) side, thereby, realizing interdigitated contacts for the absorber and emitter point contacts. The result is shown in Figure 1d and f). The above mentioned isolation scribing combined with the metal patterning results in an interconnection scheme with cells being monolithically series connected to modules. By contacting contacts A and B (Figure 1f), it is possible to measure cell 1, while by contacting A and C, it is possible to measure cell 1 and 2, connected in series. Average efficiencies above 9% were measured on these mini-modules (see deliverable report D9.17). Those results were achieved without the incorporation of light-trapping concepts as developed in task 9.1.

2.1. Innovative and scalable interconnection scheme using tunneling contacts

An alternative contacting scheme has been designed and tested by EPFL in the form of mini-modules comprising serially interconnected narrow cells. Narrow cells are required due to the high sheet resistance due to the low thickness of the LPC Si absorber. To simplify the back contacting of the cells and it related process, a tunneling concept originally developed for interdigitated back contacted (IBC) c-Si cells was used.

The tunneling contact concept shown in Fig. 2 comprises the patterning of one doped contact and then the deposition of another doped contact over the entire back surface without patterning it. The scheme thus reduces the number of patterning steps and avoids the need of alignment of the second type of doped contact to the first one. It is therefore very attractive for LPC Si cells and permits the use of cost effective patterning methods (in particular no need for photolithography). This concept was validated on mono c-Si based cells with a 9 cm^2 cell area and an efficiency >22.5% [6].

Using this tunneling concept, an interconnection scheme as detailed in Fig. 3 was designed. One can see that only the a-Si:H(i)/µc-Si:H(p/n) layer is patterned. All patterning steps are performed on a glass substrate fully covered with the LPC-Si layer. This scheme involves only scalable processing steps. The process flow, after the deposition and crystallization of the absorber on the glass superstrate, is the following:

[5] M. Weizman, H. Rhein, K. Bhatti, R. Duman, C. Schultz, M. Schüle, O. Gabriel, S. Ring, S. Kirner, C. Klimm, M. Nittel, S. Gall, B. Rau, B. Stannowski, R. Schlatmann, and F. Fink, “Rear-side All-by-Laser Point-contact Scheme for liquid-phase-crystallized silicon on glass solar cells,” Sol. Energy Mater. Sol. Cells, vol. 137, pp. 280–286, Jun. 2015.
[6] A. Tomasi, B. Paviet-Salomon, Q. Jeangros, J. Haschke, G. Christmann, L. Barraud, A. Descoeudres, J. P. Seif, S. Nicolay, M. Despeisse, S. De Wolf, and C. Ballif, “Simple processing of back-contacted silicon heterojunction solar cells using selective-area crystalline growth,” Nat. Energy, vol. 2, no. 5, p. 17062, 2017.

- Laser patterning of the absorber
- texturing of the LPC-Si in alkaline solution
- surface cleaning (Piranha + RCA2)
- Deposition of an a-Si:H(i)/µc-Si:H (p/n) stack (minority contact formation)
- Hot-melt patterning by ink-jet
- surface cleaning (Piranha + RCA2)
- Wet etching of the a-Si:H/µc-Si:H stack
- Hot-melt stripping
- Deposition of µc-Si:H (n/p) layer
- Deposition of a TCO/Ag layer stack
- Hot-melt patterning by ink-jet
- Wet etching of the TCO/Ag stack
- Hot-melt stripping

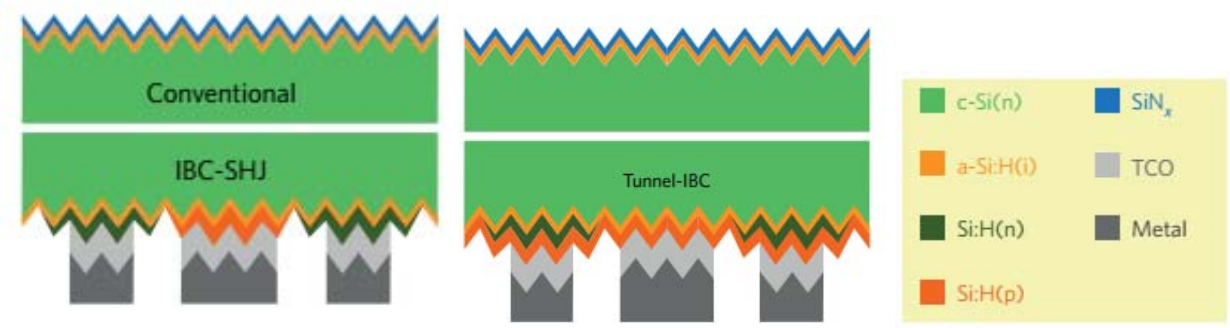


***Figure 2**. Schematic view of a conventional IBC cell and the tunnel IBC cell (IBC cell with tunneling heterocontacts. From [6].*

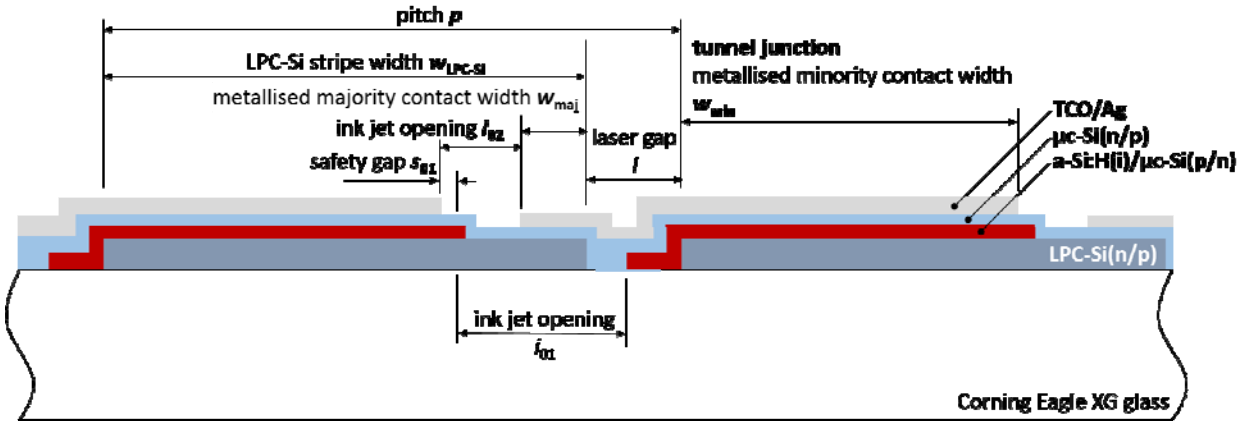


***Figure 3**. Interconnection scheme for LPC Si cell with tunneling back-contacts.*

Test devices with several mini-modules of 10 cells have been fabricated on 5x5 cm^2 glass substrates. The design comprises cells with various pitches (600 – 1200 μm) and, as a consequence, various cell widths. For all pitches two different back-surface field (BSF) ratios (10% and 20%) were realised. It also comprises transmission line measurement (TLM) structure for contact measurements (cf. Fig. 4). Dimensions of the cell structures (see also Fig. 3 and indicated in Table 1). Pictures of a fabricated module are shown in Fig. 5 while detailed optical microscopy pictures of the interconnection are shown in Fig. 6 after the first patterning step as well as on the finished module.

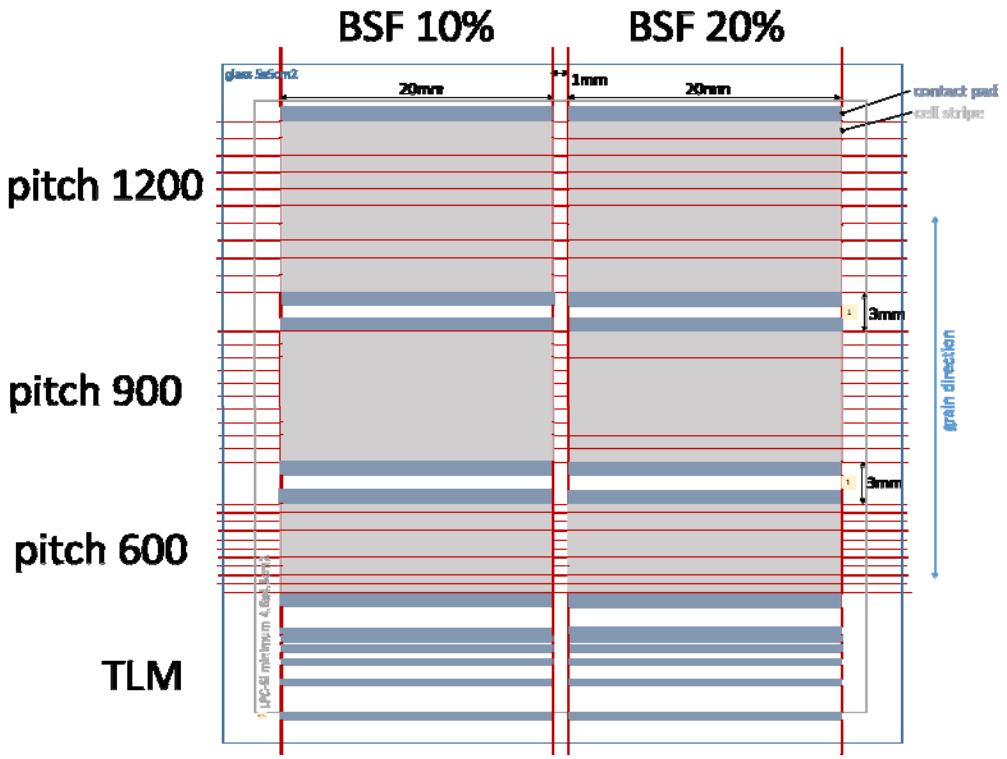


***Figure 4**. Overall test device structure with 5 mini-modules of 10 cells and TLM test structures on a 5x5 cm^2 substrate. See text for details.*

***Table 1**. Feature size of the mini-modules as defined in Fig.3 and 4. Other dimensions are: S_{01}=50 µm, i_{01} = (var), i_{02}=100 µm (S_{01} + 50 µm), l=200 µm*

	10% majority contact share (BSF)				*20% majority contact share (BSF)*			
p (µm)	w_{LPC-Si} (µm)	A_{module} (cm^2)	w_{min} (µm)	w_{maj} (µm)	A_{min}^* (%)	A_{maj}^* (%)	w_{min} (µm)	w_{maj} (µm)	A_{min}^* (%)	A_{maj}^* (%)
1200	1000	2.4	800	100	66.7	8.3	700	200	58.3	16.7
900	700	1.8	530	70	58.9	7.8	460	140	51.1	15.6
600	400	1.2	260	40	43.3	6.7	220	80	36.7	13.3

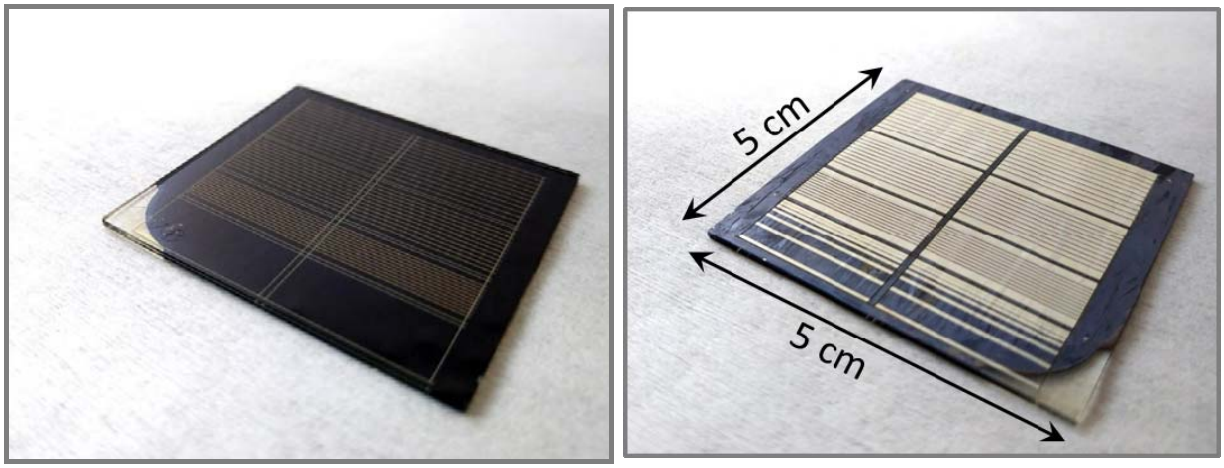


***Figure 5**. Picture of the fabricated device: Glass superstrate (front) side on the left and back contact side on the right.*

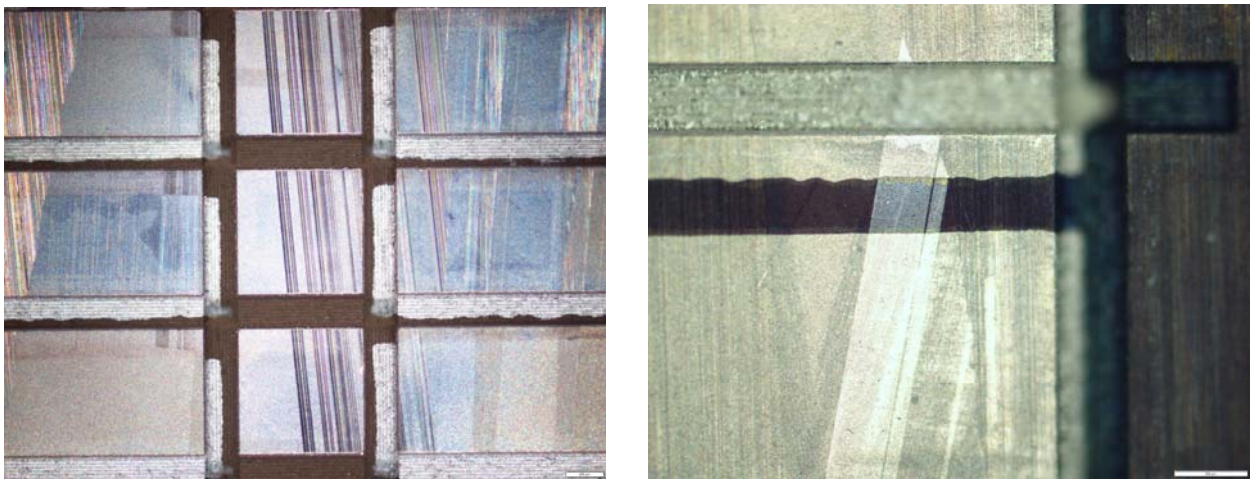
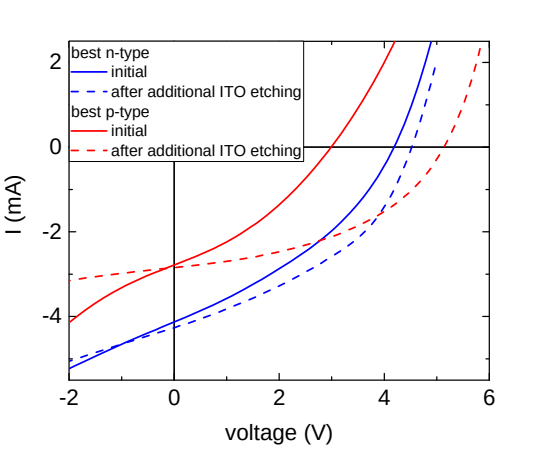


***Figure 6**. Detailed picture of the interconnection regions between two mini-modules (center of the substrate after the first hot-melt patterning step (left) and zoom-in on the finished device. (right).*

IV characteristics and view of the realized devices are shown in Fig. 7. All modules were working but exhibited low shunt resistance, most probably due to the presence of residual ITO between the cells. The ITO was deposited at room temperature but the substrates heated up to a temperature of 170°C during Ag deposition by sputtering. At this temperature, ITO becomes crystalline and difficult to etch. Additional etching was able to remove part of this ITO and to increase the shunt resistance. Some difficulties were also encountered to etch the µc-Si(p) layer. Both etching processes should be further optimized to achieve much higher shunt resistance and therefore higher efficiency. IV curves simulations with a two diode model taking into account the observed shunts are compatible with a full area module efficiency of 8.3% (9.9% with respect to the LPC-Si area, 12.4% with respect to the minority contact area). However, these results both validate the use of tunneling contacts for LPC Si cells and interconnection scheme and indicate that mini-modules can be fabricated using scalable and cost-effective processes.



	V_{OC} (V)	I_{SC} (mA)	*FF* (%)	η* (%)
p-type	5.1	2.8	44.5	2.7
n-type	4.5	4.3	40.3	3.2
simulation	6.3	4.2	75.0	8.3

*** full area efficiency**

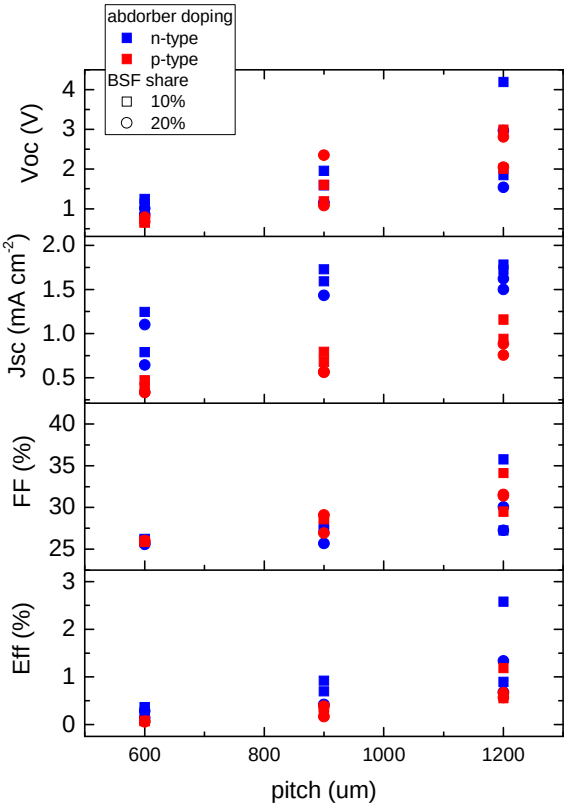


***Figure 7**. IV curves of the best devices (1200 µm pitch) in the initial state as well as after additional ITO layer etching (top left), extracted I(V) parameters (bottom left) and results performances of all mini-modules (right). Simulation results (bottom left) were obtained using a two diode model and observed shunt-resistance. The full area of the module corresponds to 2.4 cm².*

2.2. Direct laser lithography

A possible alternative way for patterning cells (for IBC or module interconnection) was developed by Jülich. It involves direct laser lithography that allows the structuring of photoresists by scanning over the light sensitive polymer material with appropriate wavelengths in the ultra-violet region. The advantage of this technique over traditional photolithography is that it does not require a complex optical setup or expensive photomasks to pattern the resist hence it is a cost effective, contactless, scalable process which allows flexibility in pattern design for research applications.

By adjusting the laser pulse peak fluence of the focused Gaussian beam we achieved lines with a width less than 25µm, lower than that of the beam radius (see Fig. 8: left) in negative

photoresist AZnLof-2020. The laser beam was sequentially scanned over the resist and the adjacent lines were merged together into broader areas as shown in the schematic in Figure 8 (right).

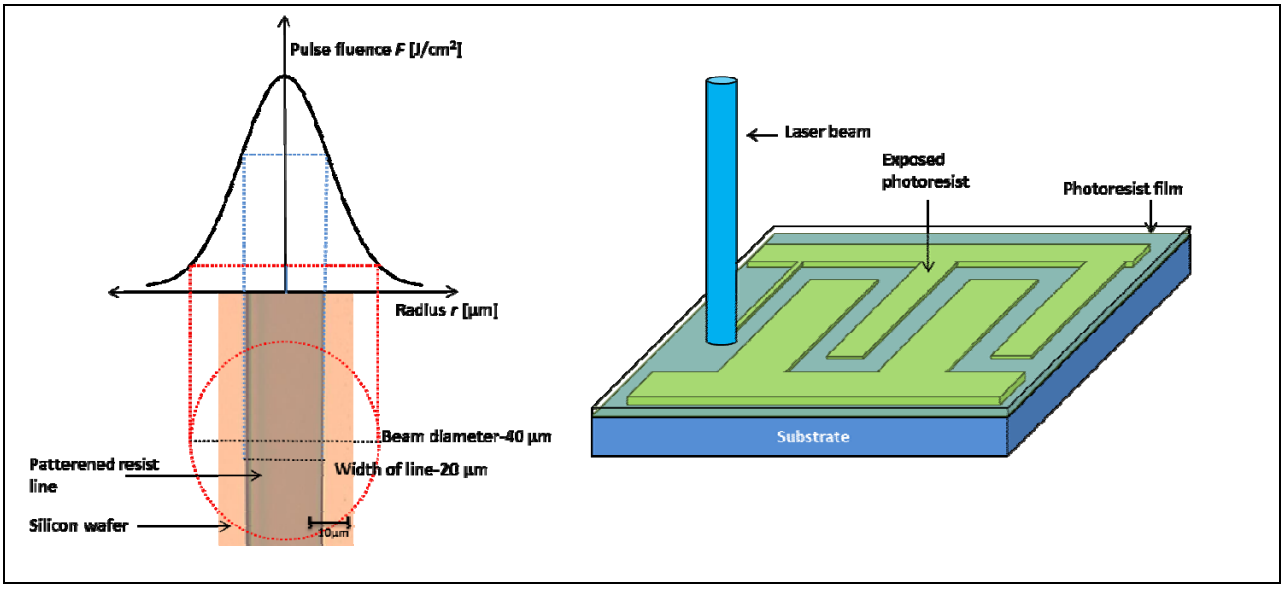


***Figure 8**: (left) Schematic sketch of pulse fluence distribution of Gaussian beam juxtaposed over light-microscope image of patterned resist line. By adjusting the fluence of the focused beam it was possible to achieve lines with lower width than the beam radius. (right) Schematic showing the patterning process of the resist coated on silicon surface using the laser beam.*

Using this process we etched silver and ITO for the purpose of making contact pads for transfer length measurements of liquid-phase crystallized (LPC) silicon on glass substrates. The samples were provided by our partners at HZB. The same processing sequence can also be used to make interdigitated back-contacts for LPC based solar cells

3. Summary

The present efficiency of LPC-Si mini-modules is far from the target efficiency of 12% as defined for this deliverable and therefore not achieved.

However, significant progress has been achieved with the validation of a simple interconnection concept using tunneling contacts. Taking into account the present losses induced by the shunt resistance, a full area efficiency of 8.3% (12.4% minority contact area efficiency) was estimated by simulation. This low shunt resistance originates from remaining TCO between the individual cells of the mini-modules. Process optimization is expected to greatly improve these results. Further module improvements are also expected with the introduction of light-trapping schemes (front and back absorber texturing) as well as possible replacement of the Ag layer with white dielectric back reflector. Direct lithography has also been applied for the patterning of IBC LPC-Si cells. It is a promising scalable and cost effective method that could also be applied in the patterning steps for the interconnection. Finally, we should note here that LPC-Si development was only started in Cheetah at mid-term and that the timeframe for these developments (at Jülich and EPFL) was only two years.