Europe's Research and Development efforts in support of its PV industry

European Solar Technology Forum
From Research to Industrial Application
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This project has received funding from the European Union's Seventh Programme for research, technological development and demonstration

Wafer based Crystalline silicon - "Getting below a 100 microns"

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This project has received funding from the European Union's Seventh Programme for research, technological development and demonstration

Objectives and motivation (CHEETAH)

Demonstrate the feasibility of making thin wafers/foils and processing them into cells and modules.

Cost reduction of around 20% compared to current module technology: < 0.5 €/Wp and improved environmental profile.

Motivation:
Enhance the implementation of solar energy by cost reduction.

Impact of the results:

Short term: Industrial equipment suppliers for cell and module technology can develop and promote their equipment for application to thin-cell based modules.
Long term: Cost reduction of PV by use of thinner and kerfless (epitaxially grown)wafers.

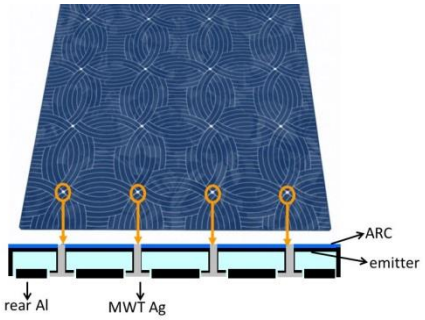
Two high efficiency platforms for cell and module

Thin c-Si cut wafers

thin c-Si epi wafers

Thinnest SHJ cells

Back Contact foil based (BC)



Labscale production
80-100 µm

Thin IBC cells

Thin IBC modules

Standard Hetero Junction (SHJ)

Thin SHJ cells

- Large numbers for modules and highest record efficiency
- By existing equipment
- Industrial pilot production
- 80-100 µm

Thin SHJ modules

Tabbing/stringing
(conductive adhesive)

Why thin wafers / foils ?

A combination of cost and efficiency !

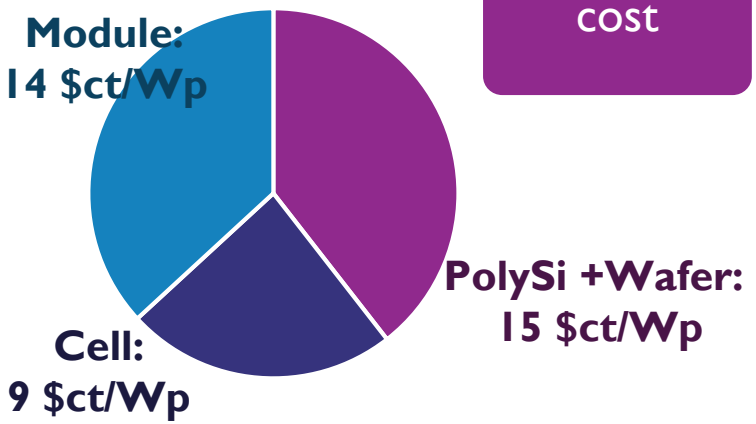
Cost Si wafer is > 30% of total module cost

(current common thickness 180 um)

Solar cells on thin c-Si wafers

Reduced cost

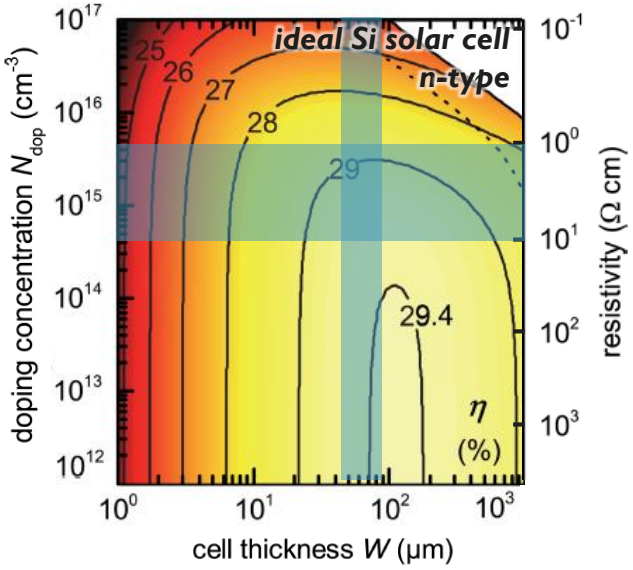
Increased efficiency



ITRPV, March 2017

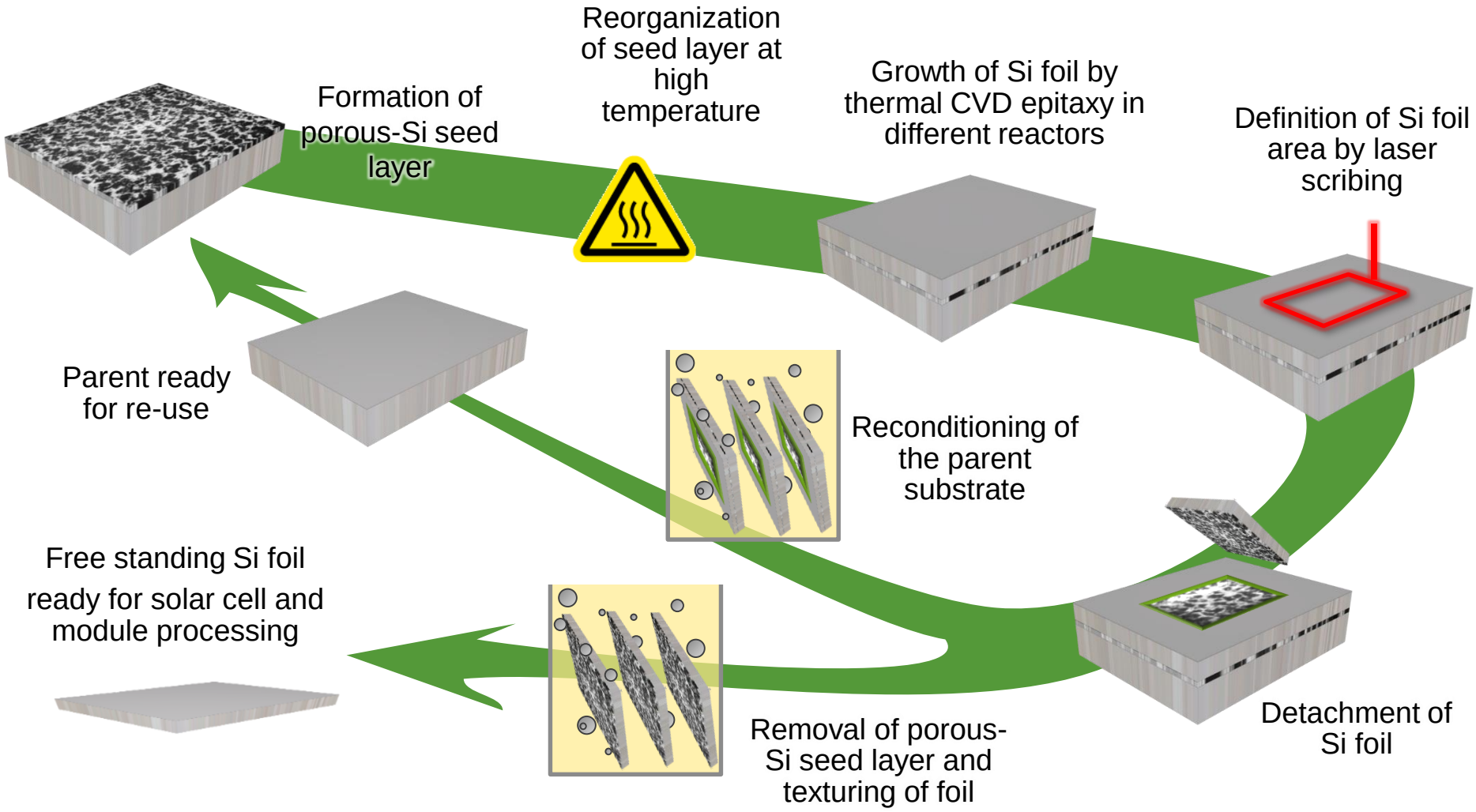
Theoretical max η for 50-100 µm

(for common base doping of 1-10 Ohm.cm)



Richter et al., IEEE Journal of PV (2013)

Fabrication of epitaxial foils

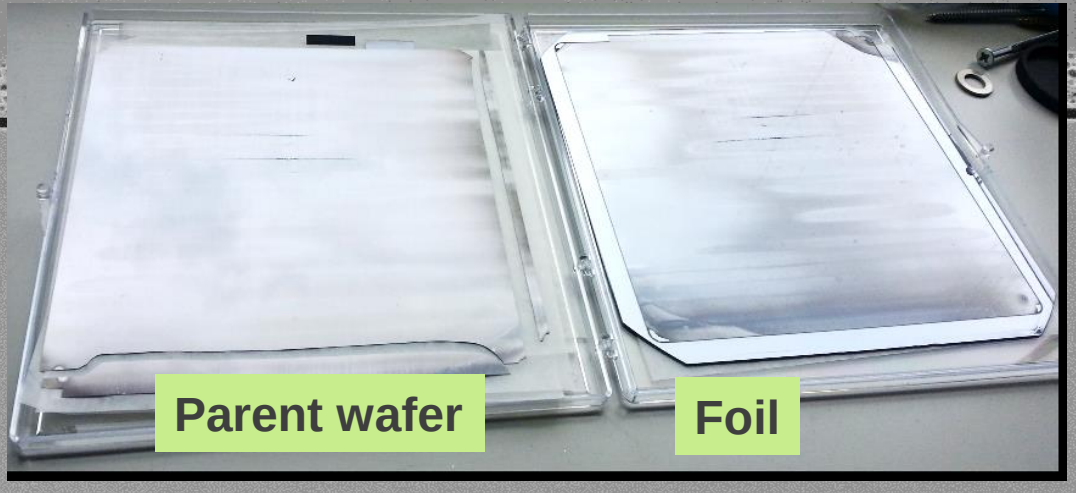


Fabrication of epitaxial foils in high-throughput tools

ProConCVD (inline CVD tool) and
Inline porosification tool (right).

High-throughput tools

NexWafe is commercialising EpiWafer



12.5x12.5cm 85um-thick foil and parent

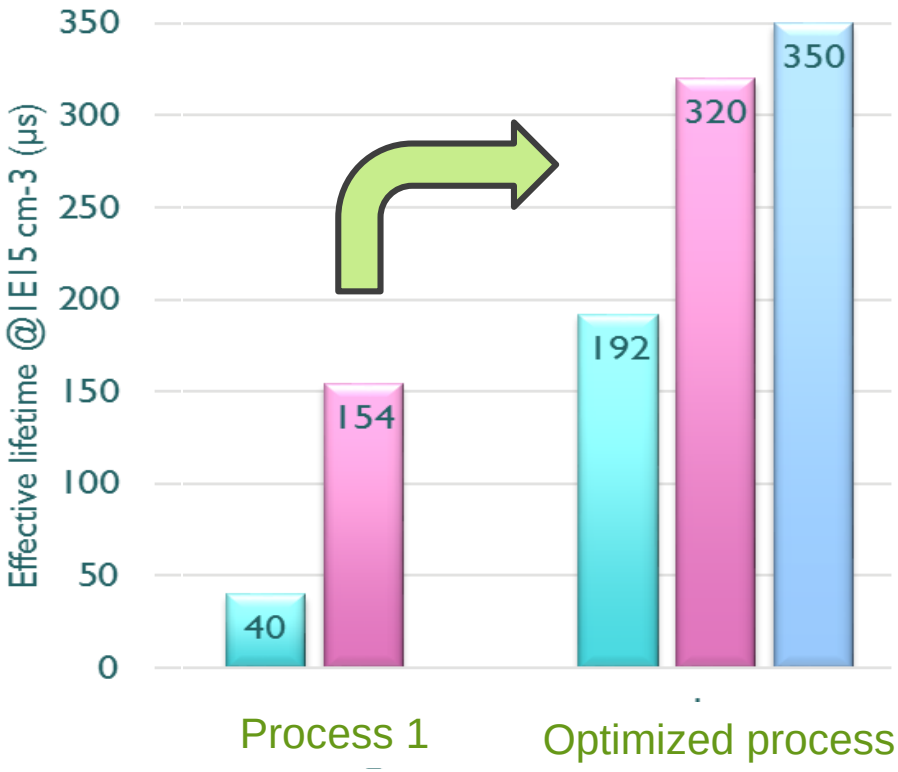
Epitaxial foil (X-SEM)

Low porosity layer

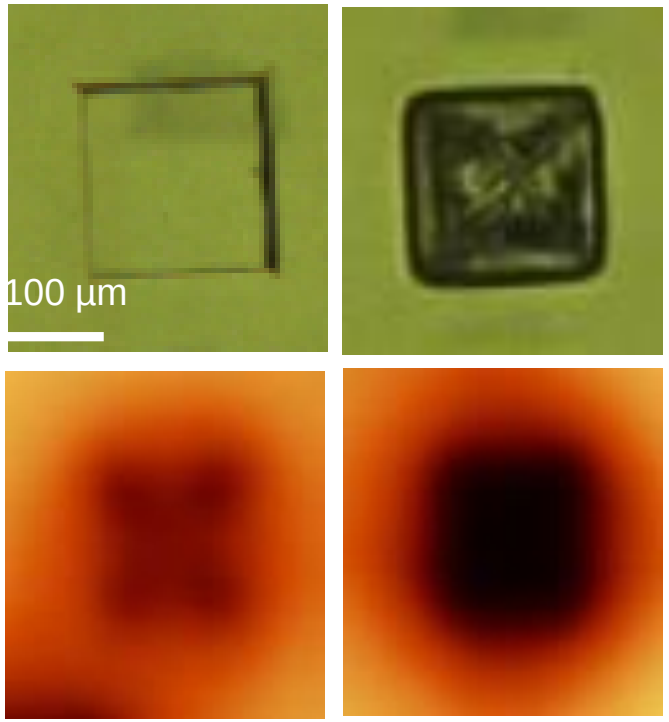
High porosity layer

Parent substrate

Improved understanding to increase material quality



Effective lifetime (µs) of 40µm epitaxial foils for 2 different growth processes.



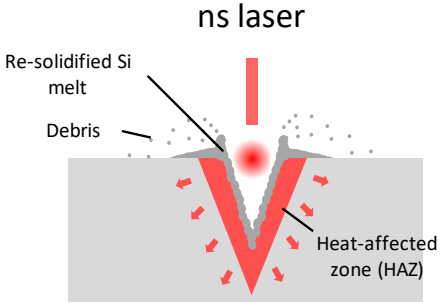
Optical micrographs (above) and lifetime mapping (bottom) of growth defects.

Improved understanding in crystalline defects in epitaxial wafers/foils.

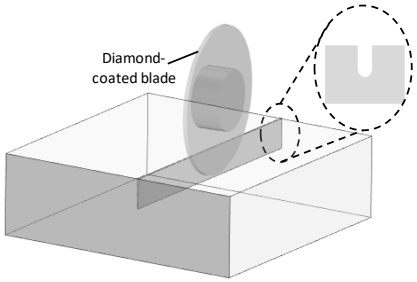
Optimization of growth process to improve effective lifetime of epifoils.

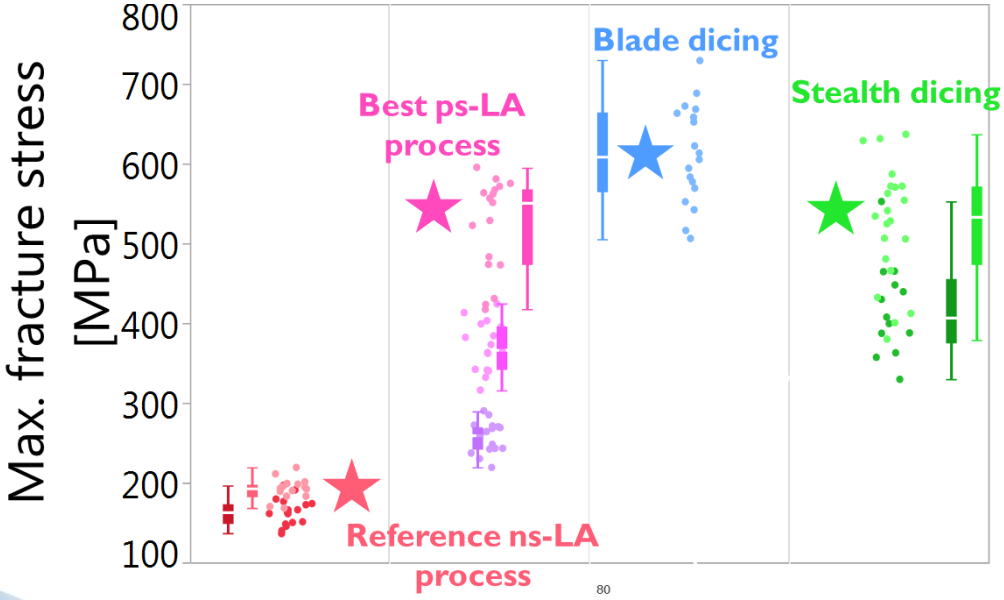
Detachment and edge definition

ns laser ablation

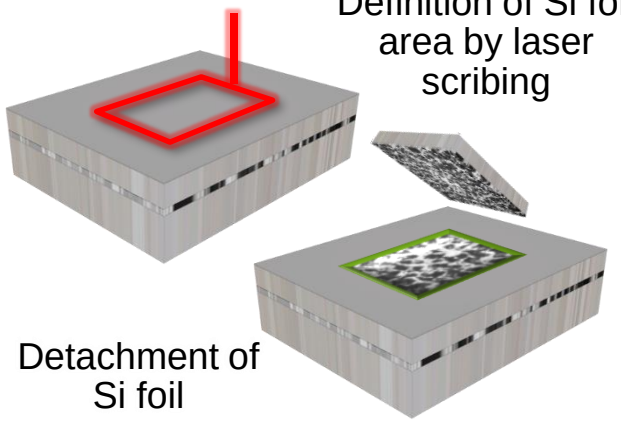


Blade dicing





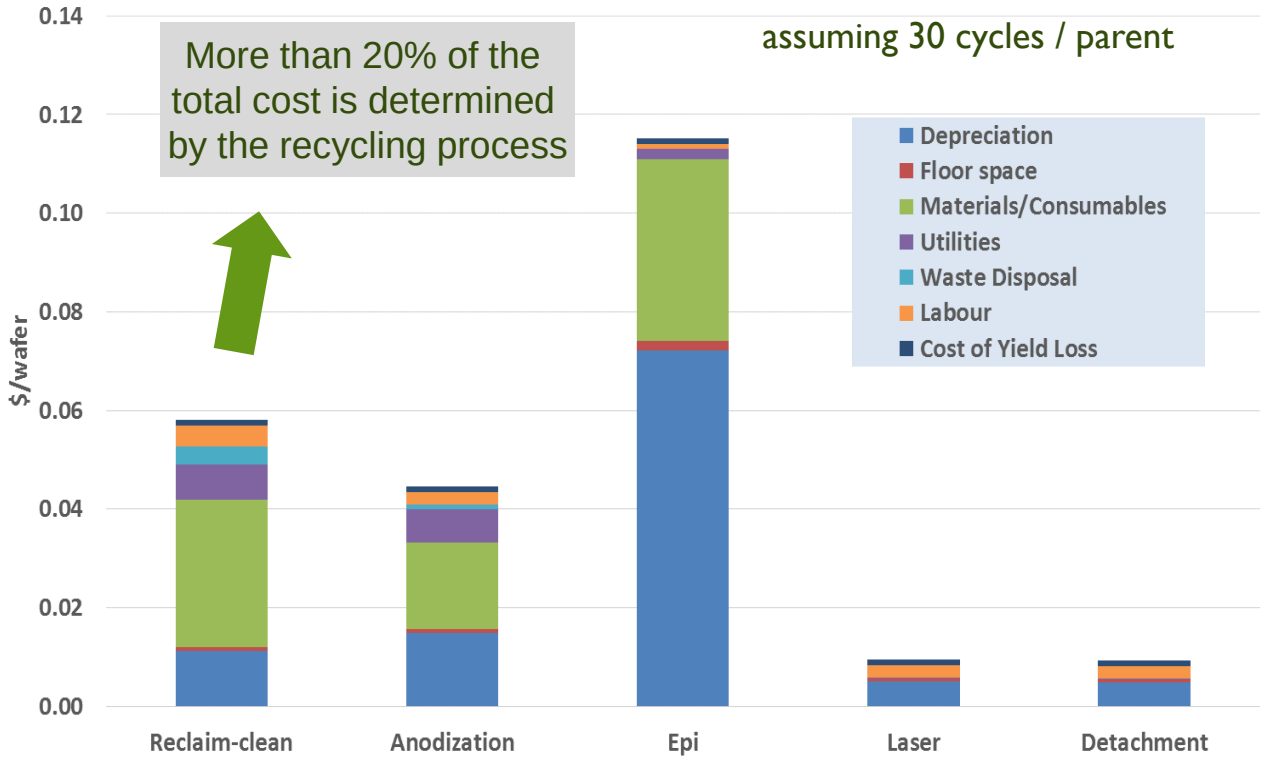
Edge definition and detachment method determine mechanical stability of foils and very thin wafers.

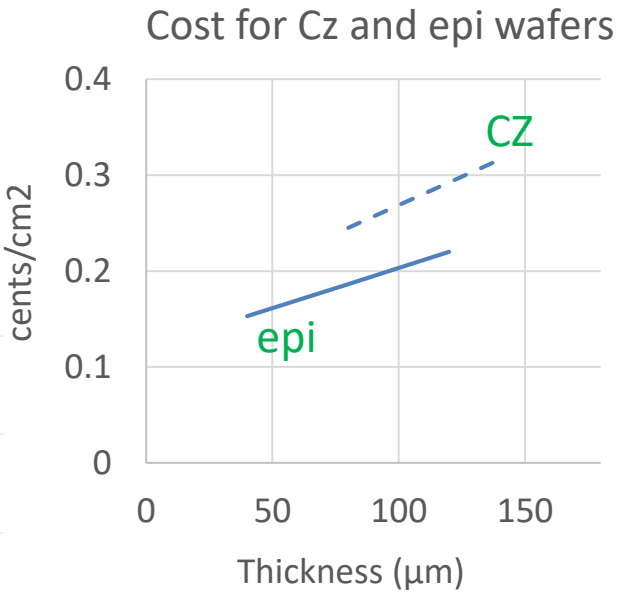


Recycling of parent substrates

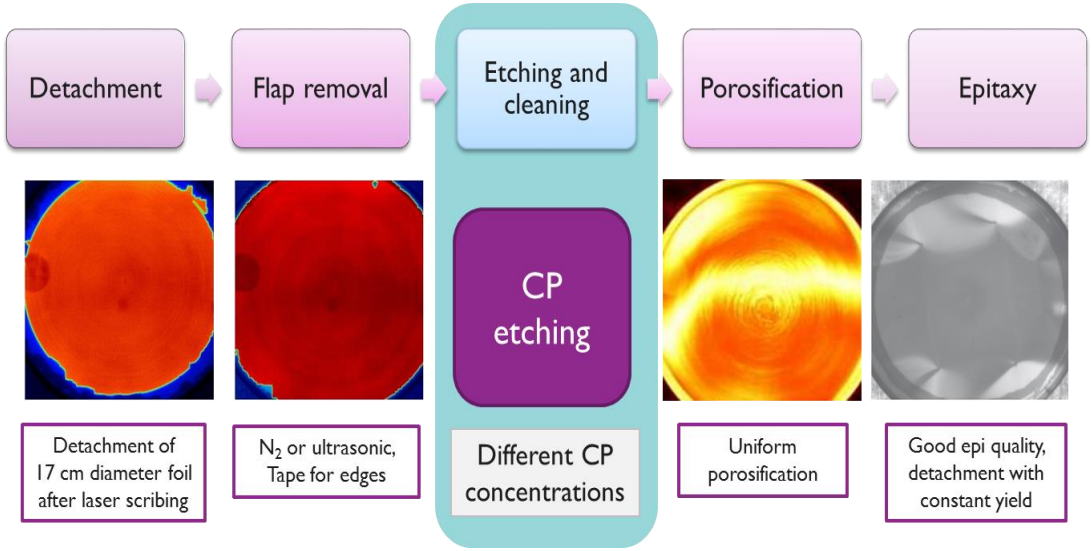
Motivation

Recycling of the parent substrate is needed to make epifoil fabrication cost effective.

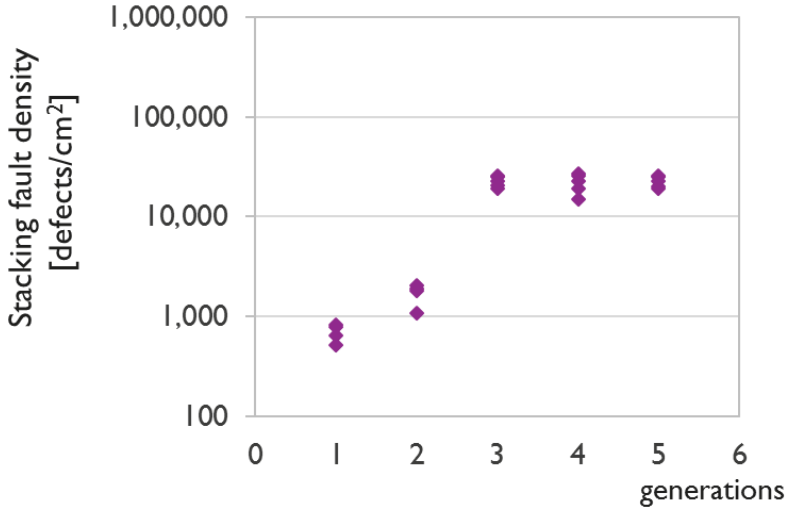




Recycling of parent substrates



Stabilization of the foil quality for higher generations



CHEETAH:
- Recycling for 5 generations is demonstrated by wet etching
- CVD and Psi set-ups need to be adjusted to recycling process

Literature:

Univ. Stuttgart : **13x** (P. Kapur, proc. 28th EUPVSEC)

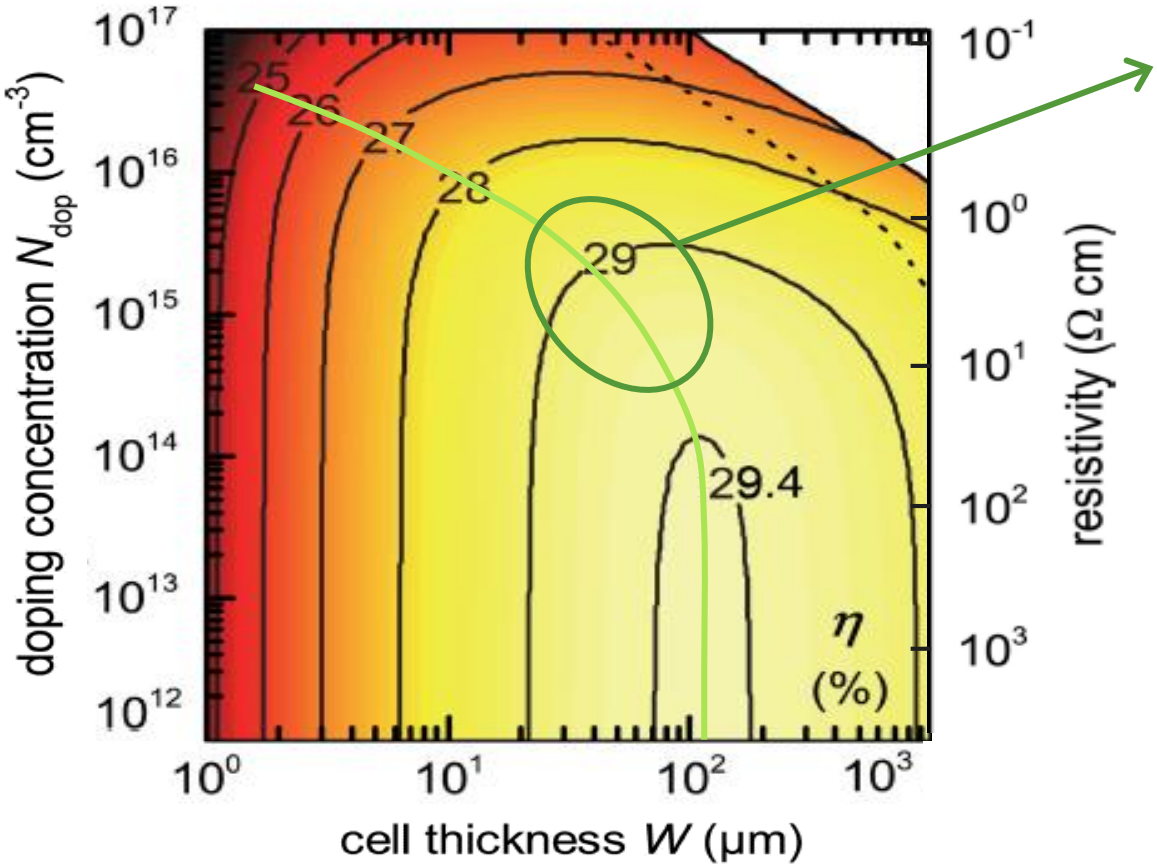
Crystal Solar: **50x** (R. Horbelt [proc 31rst IEEE 2005]

Solexel: **50x** (Verena Steckenreiter [IEEE Journal of Photovoltaics, 6(3):783–790,2016])

Recycling process developed in several institutes/companies.

Cell performances vs substrate thickness

ideal Si solar cell n-type



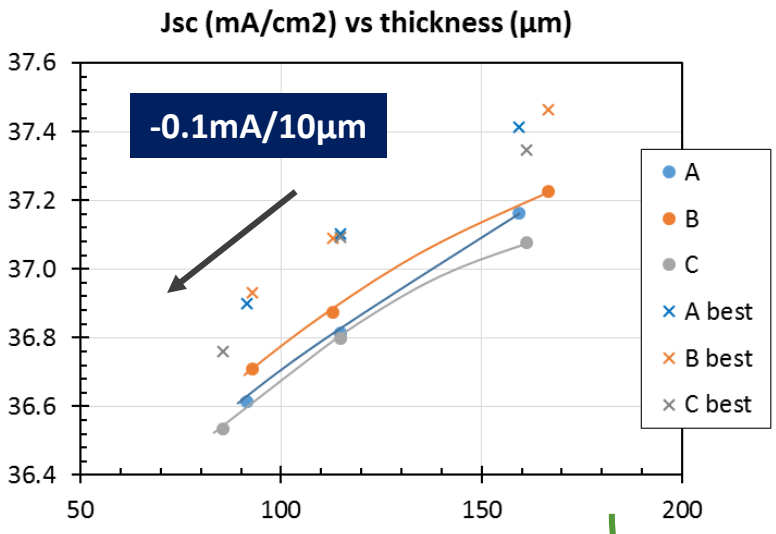
Optimal performances in the 20 to 100µm range for common resistivity : **is it really the case in practice ?**

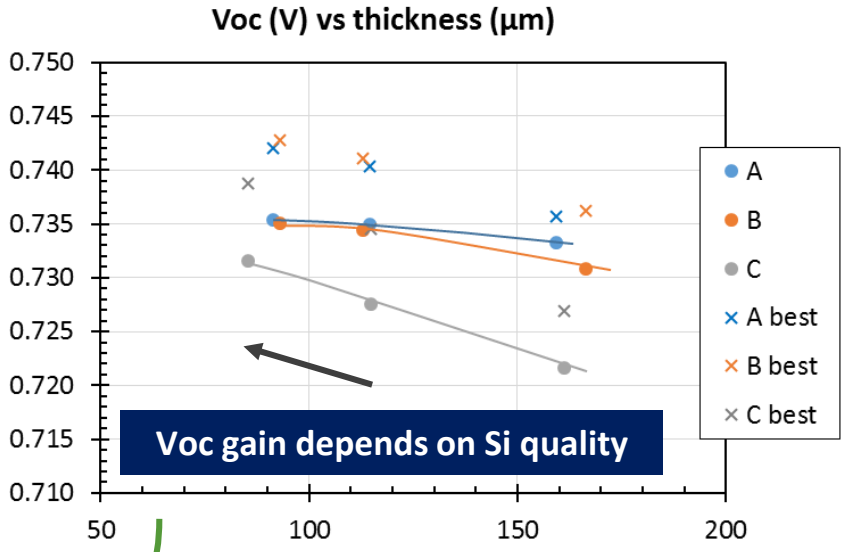
- CHEETAH focused on Si Heterojunction cells because of apriori easy process integration (low T° + front & rear side symmetry) and high efficiency potential (Voc !) well demonstrated by Panasonic, Kaneka, Choshu …

Richter et al., IEEE Journal of PV (2013)

SHJ performances vs thickness

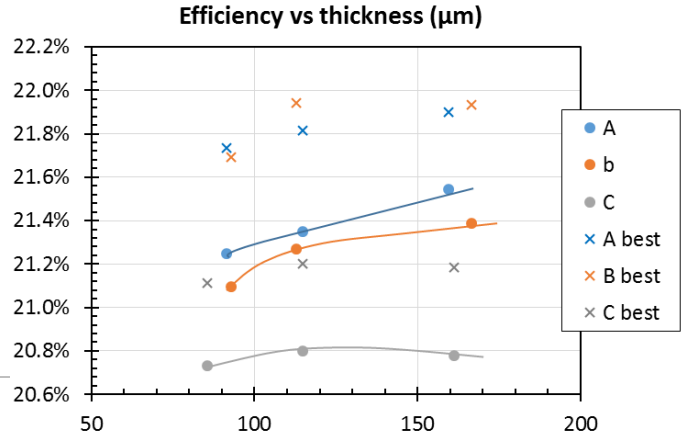
Current non-ideal cells and substrates ! Si quality A = B > C





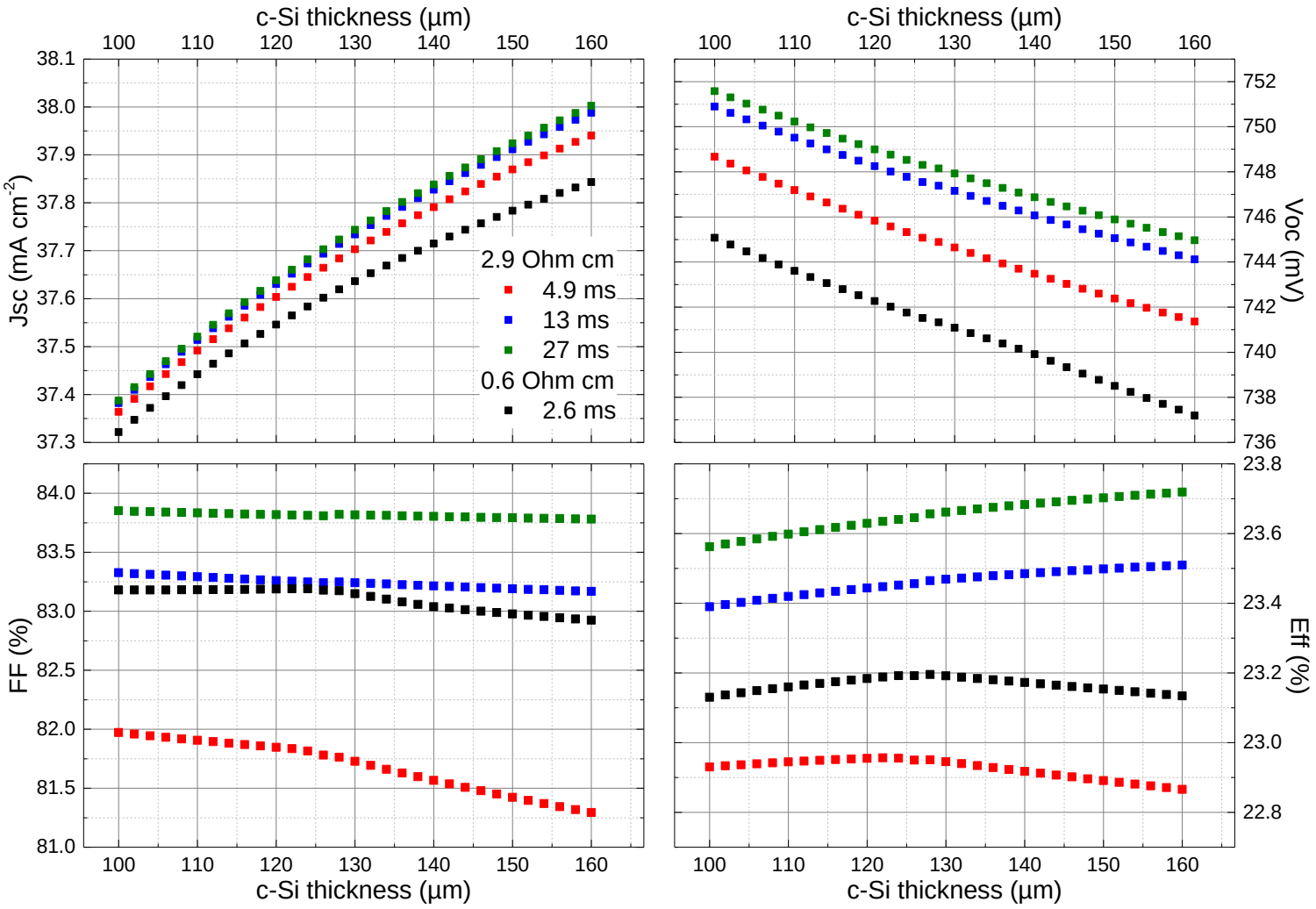
Thin wafers :

- ✓ **SHJ OK with same processes down to 80µm**
- ✓ **Voc & Jsc balance : Efficiency almost stable down to 100µm and some benefit for low quality Si = additional gain in overall production costs**
- ✓ **Current record cell : 22.2% @ 89µm (4BB, bifacial, 156x156 full industrial integration on CEA pilot line)**



Simulation

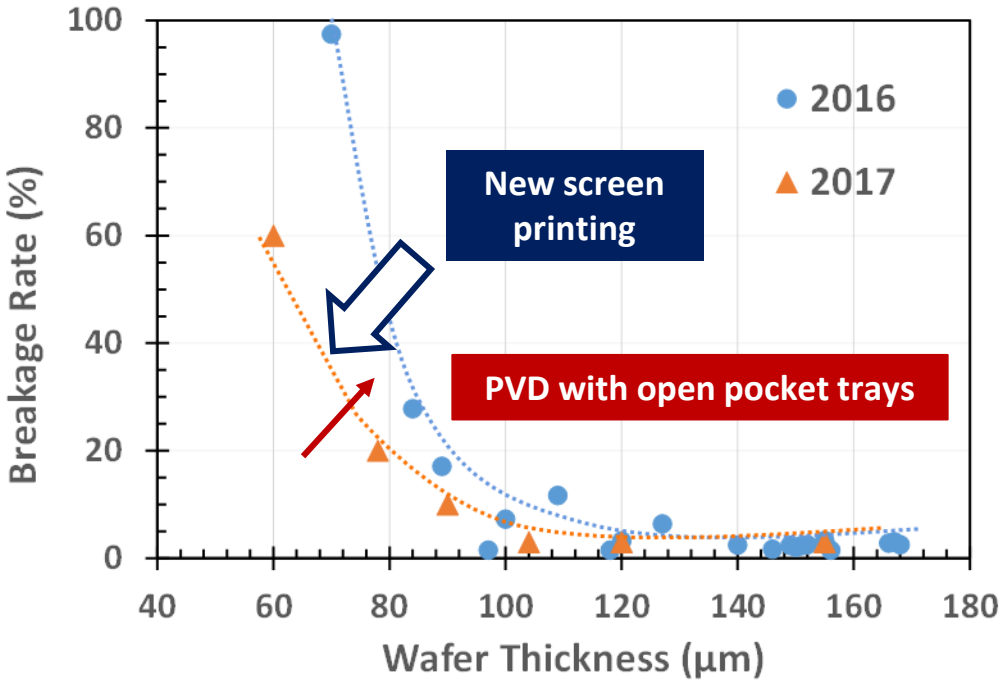
Non-ideal SHJ cells



- ✓ **Very good agreement with practical data**
- ✓ **From cell / module perf. Point of view: 100µm is fully OK TODAY …. and might be even better in the future**

Breakage rate and defectivity

SHJ pilot line: industrial equipments

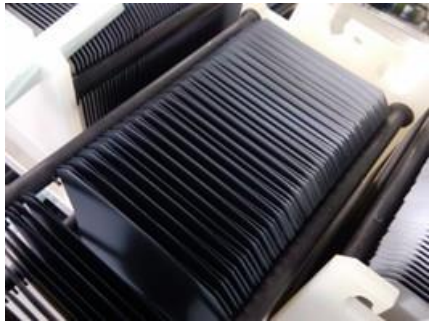


Iterative learnings and optimization of current automation (cassettes, pickers, belts, trays …)

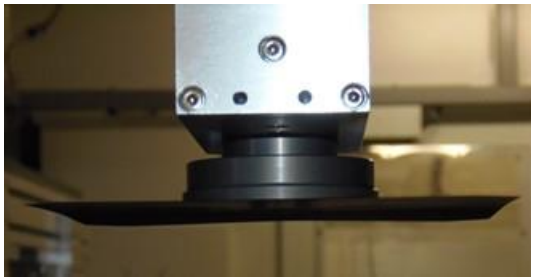
- Overall defectivity & breakage rate has been improved for 160 – 80µm (full auto) and 80 – 40µm (semi auto) cells

- Less defectivity → improved cell efficiencies
- Less breakage → improved throughput, higher number of working cells
- Possible to integrate in quasi full-automation mode ultimate wafers (Th < 70µm)

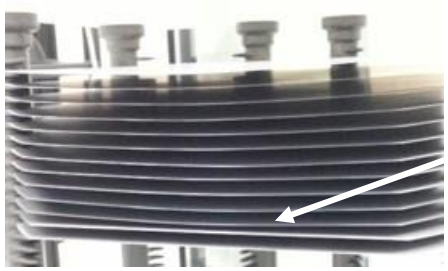
- Global breakage rate with no production line adaptation: OK until ~100µm
- New PVD with open pockets: apparition of new « electrical » defectivity for wafers < 100µm



Wafer sticking post HFLast



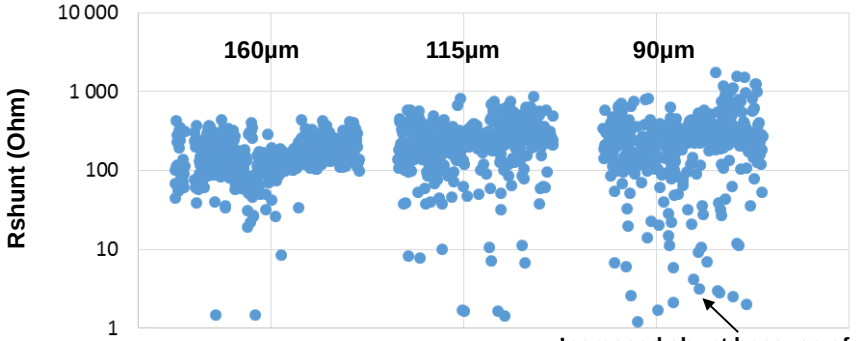
Automation + pick&place

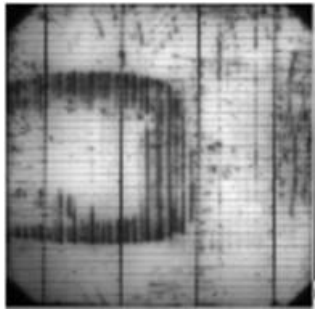


Excessive wafer bowing in cassette

Main defectivity/Breakage source!

New « Electrical » increased defectivity for lower thicknesses



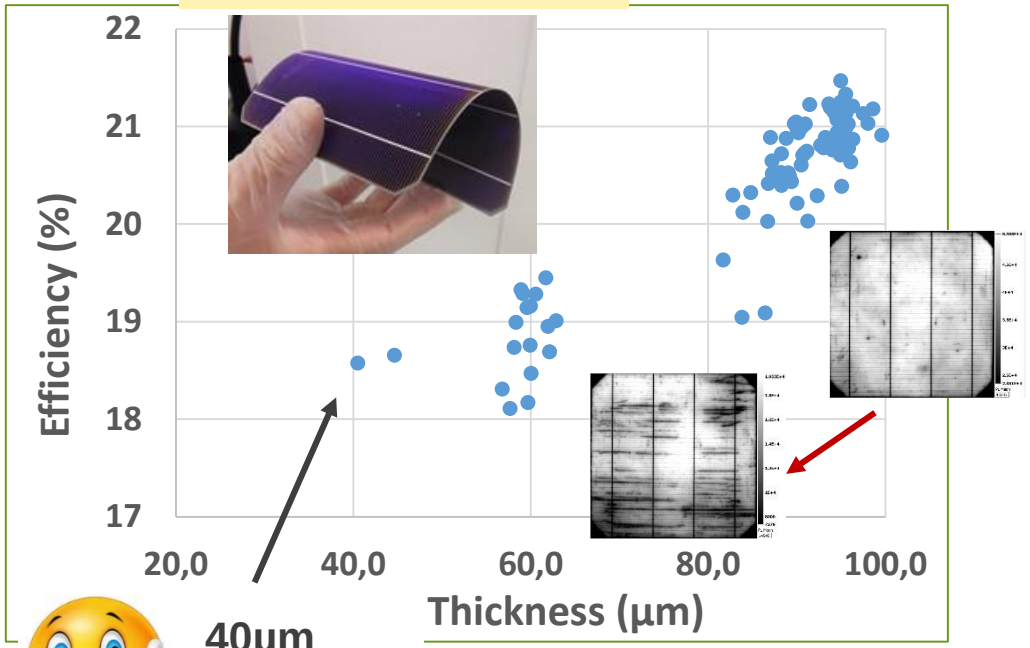


Increased friction on trays + difficulty to maintain the wafers in the tray pockets

Increased shunt because of misplacement of wafers in the PVD tray pockets

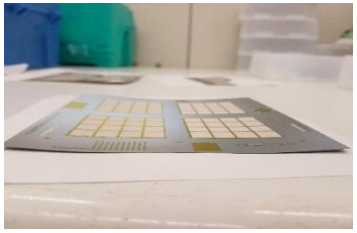
Ultimate thickness

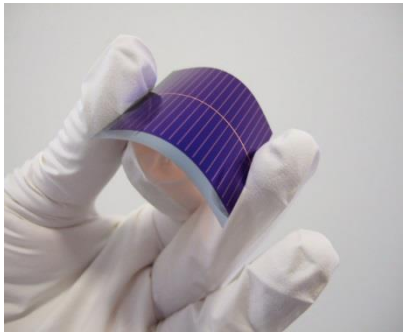
60µm SHJ bifacial cell



Th (µm)	Jsc (mA/cm²)	Voc (mV)	FF (%)	Eta (%)
Cz 40	34.7	730	73.3	18.6
Cz 45	35.1	732	72.7	18.7
Foil 40	33.5	693	73.8	17.0

40µm 156x156



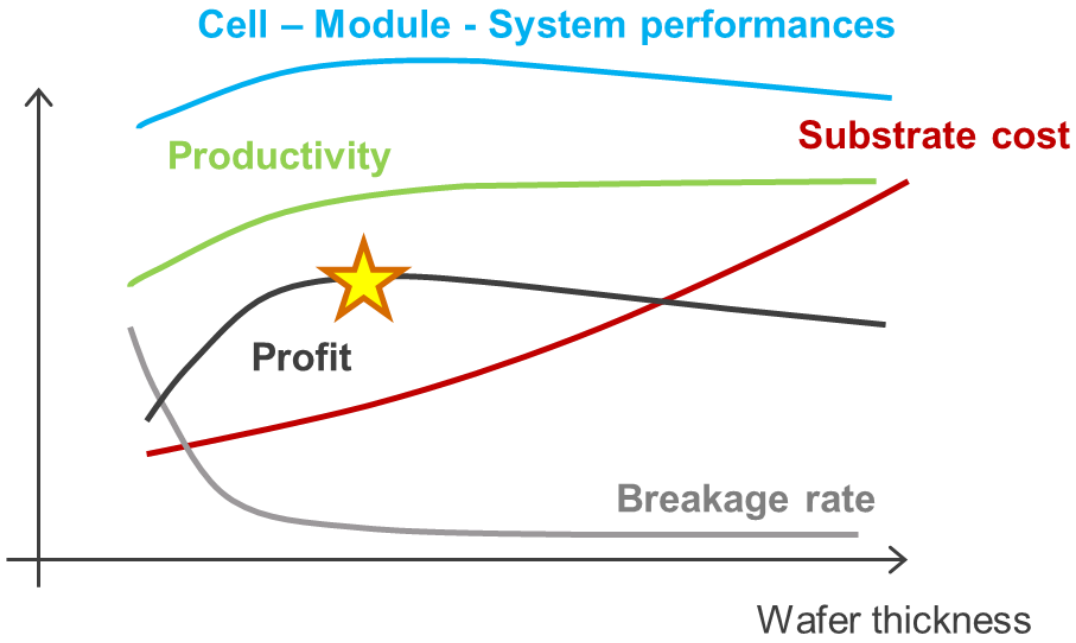


40µm 125x125 EpiFoil 4x4cm²SHJ cells

- Sudden drop of efficiency for ultra-thin wafers related to defectivity increase with not well adapted handling
- Demonstration of 40µm cells on Epifoils and on Cz wafers

Costs

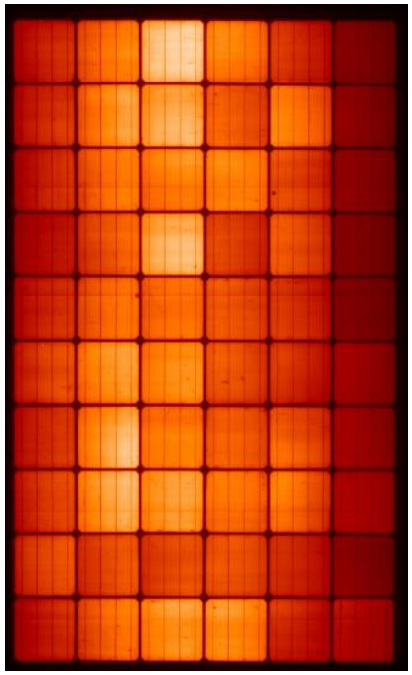
- Present technologies (carrier, belts, pickers, trays ..) can be OK down to 80 – 90µm with minor adjustment
- Specific solutions required for stand alone ultra-thin substrates (< 80µm)
- Process development specific to ultra-thin cells and module might help

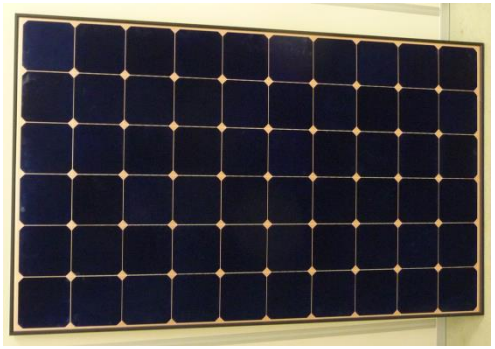


- ✓ **Combination of all inputs will give an optimum for production profit … with thinner cells !**
- ✓ **Cell and module industry can follow wafer supplier roadmap without high risk**

Module results

A few full size SHJ modules with thin cells (90-100 µm) built (INES) + (latest news!) one IBC (ECN)





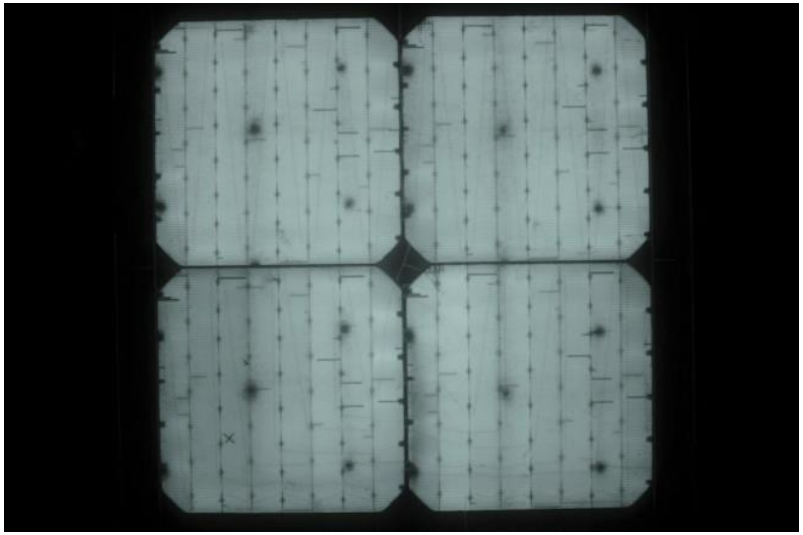
IBC 95µm 60-cell module, CTM power > 99 %

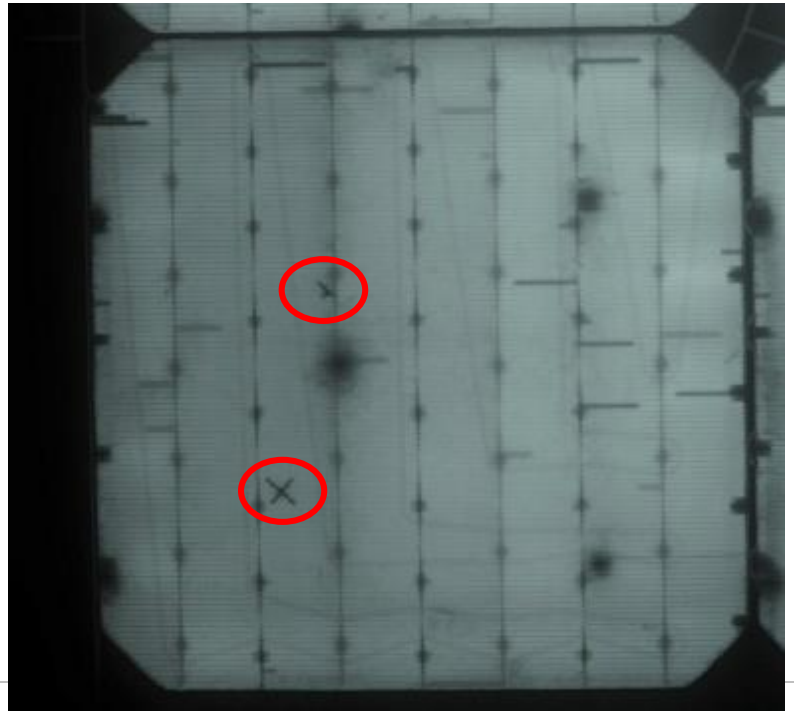
EL image of SHJ 93µm 60-cell 313 Wp record module

Module results

module integration of thin cells down to 80 µm feasible for both back contact (ECN) and tabbed modules (INES).

Formation of microcracks is more critical for thinner IBC cells during module assembly, but can be avoided by fine-tuning lamination.





EL picture of 100 µm 4-cell module and detail

Module results

Application of commercial back contact and heterojunction module assembly line to thin cells is feasible (fast pick and place process does not induce damage to cells)

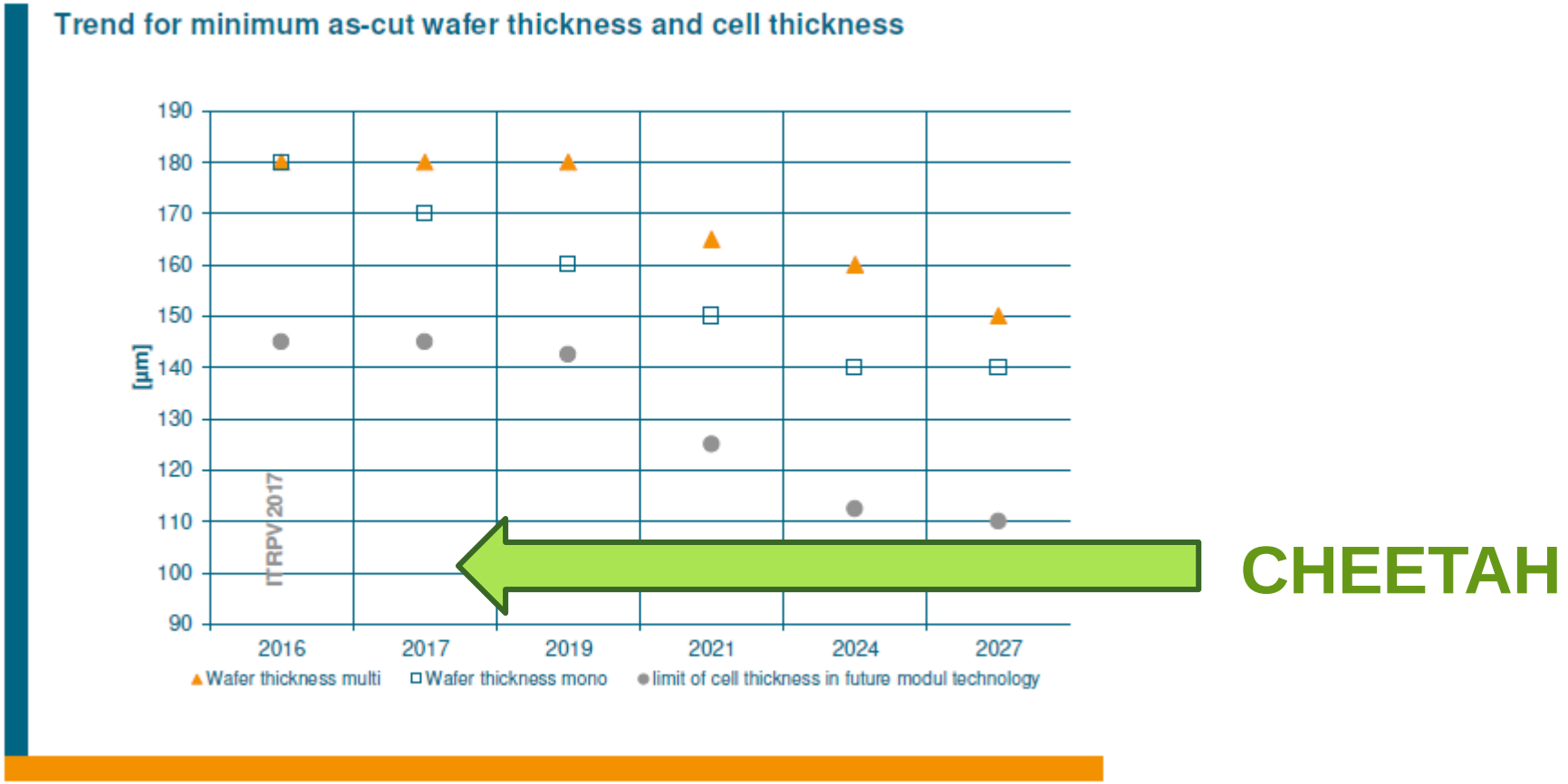
Thermal cycling (TC) test (AIT) so far not critical for thin cells:

- 4-cell back contact modules passed full TC (200 cycles), i.e. no formation of micro cracks

- Full size SHJ module (tabbed) passed TC so far (50 cycles), no formation of micro cracks

Cost reduction on module level of 18-20 % feasible using 80-100 µm epi wafers instead of 160 µm cut wafers (current price 0.8 $/wafer), all other parameters kept equal

Significance for the industry



1) Efficient 100µm cells and modules with cost benefit : proof of concept done ! 10 years ahead to ITRPV

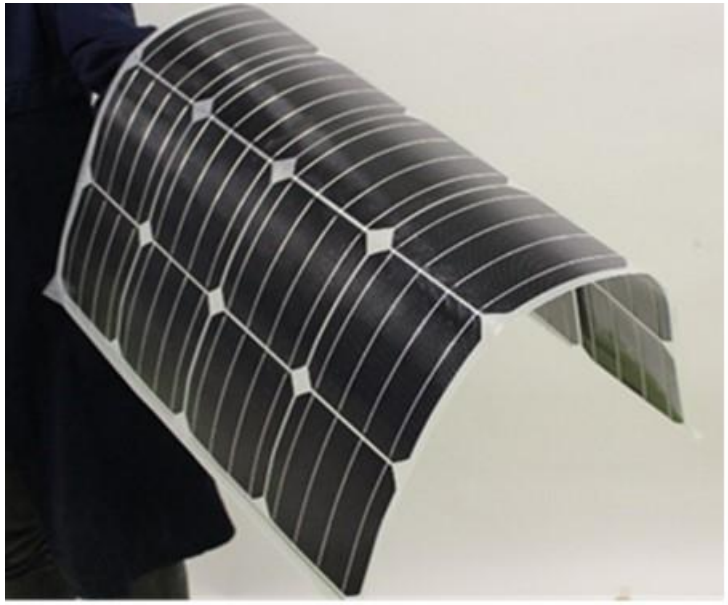
2) Better with less : 40µm integration demonstrated (cells ; Epifoils and Cz wafers).

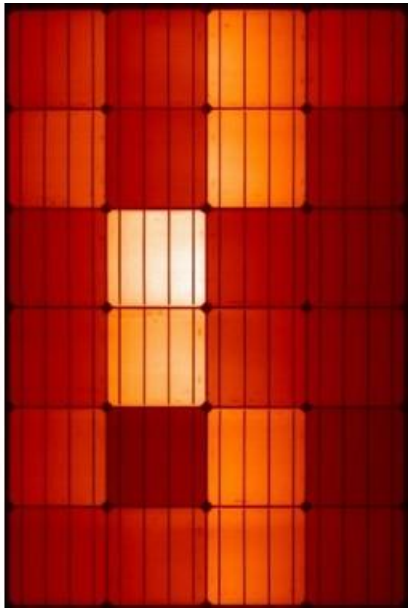
Significance for the industry

- Good opportunities for epitaxial wafer industry
- Suppliers of wafer, cell and module manufacturing equipment can develop and sell more equipment if the demand grows due to reduced PV module costs, also specific equipment dedicated to thin cell/wafer handling
- Total value chain could benefit from lower material cost (thinner wafers)
- And finally opening of completely NEW MARKETS!

Thin cells also open up new PV applications for aeronautics, space, others

Example: Light and flexible 24 Cell Module with 115µm SHJ cells





< 600g / m²

> 180W / m²

Courtesy of ThalesAlenia & CEA INES collaboration

CHEETAH

Thank you!

Any questions for our experts?

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Questions to the industry

- Do you think these CHEETAH innovations (will) matter?
- What do you think is important for short, medium and long term to further mature these innovations?
- What do you think is important for short, medium and long term for the industry to adopt these innovations?
- How could your company benefit from these innovations?
- What other innovations not investigated in Cheetah are important for the industry on short, medium and/or long term?

Back-up slides for discussions

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Cells on thin substrates: Summary table

Thickness Range	Line Status (Cell / Module)	Critical Step(s)
160µm →120µm	No Problem	-
120µm → 100µm	Minor Adjustments needed No adjustment needed for module integration	✓ Sticking during drying
100µm → 70µm	Several adjustment needed for cell integration Minor Adjustment needed for module integration	✓ Sticking during drying ✓ Adapted Automation + Handling (Slower / Adapted Carriers)
70µm → 50µm	Major Adjustment needed Not Tested @ Module Level	✓ Sticking during drying ✓ Full Manual Automation + Handling
< 50µm	Not compatible with current production line and equipment	✓ All processes