Europe's Research and Development efforts in support of its PV industry

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This project has received funding from the European Union's Seventh Programme for research, technological development and demonstration

Ultrathin wafer development and Cell processing

Pierre-Jean Ribeyron, CEA INES

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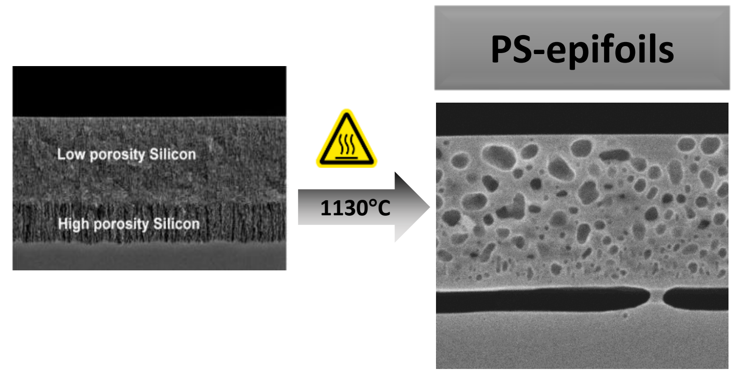
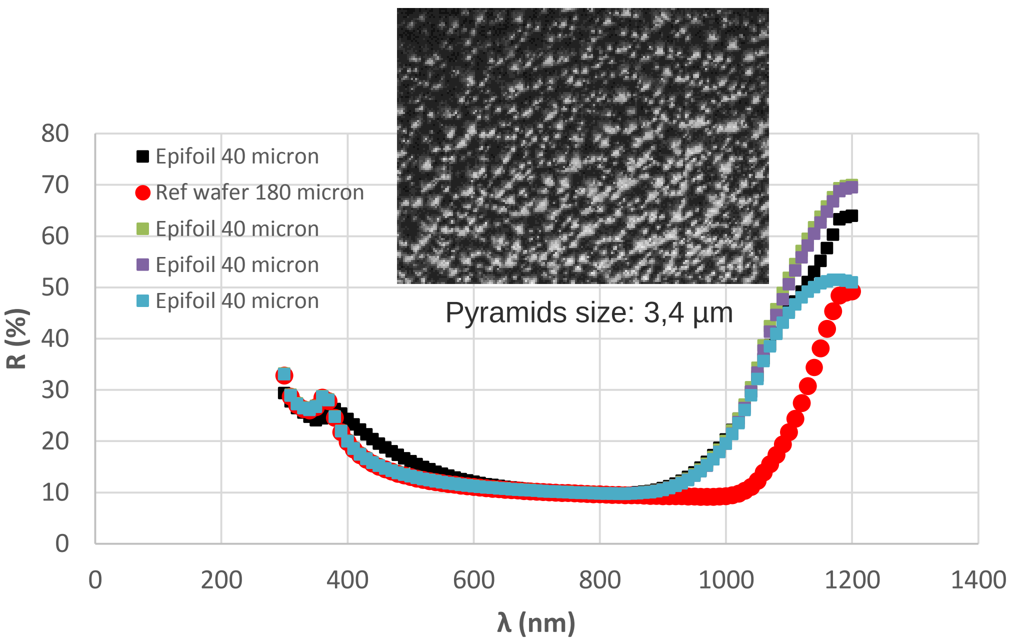
Objectives

- Development of a process for the fabrication of advanced solar cells
  - **23,5% efficiency, 2g Si/W_p and 0.3 €/W_c** on thin monocrystalline wafers ➔ 40 to 80 µm
    - Two types of 'wafers'
      - » EPIfoil (low TRL)
      - » Wire sawn wafers (high TRL)
  - Develop new technology bricks for ultra thin wafers (40 µm)
    - **Develop front side textures ➔** optical light trapping, Jsc improvement
    - **High surface passivation level ➔** Voc improvement
    - **Advanced metallization ➔** low breakage rate, Jsc and FF improvement

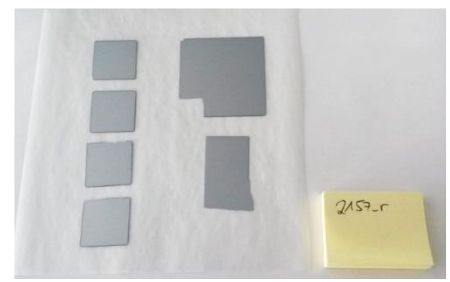
Current results on EPIfoils

- 40 µm Epifoils ➔ Front size texturing and passivation





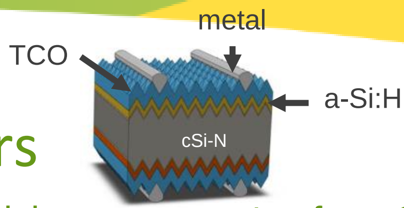
Reflectivity curve: sample without anti-reflective coating



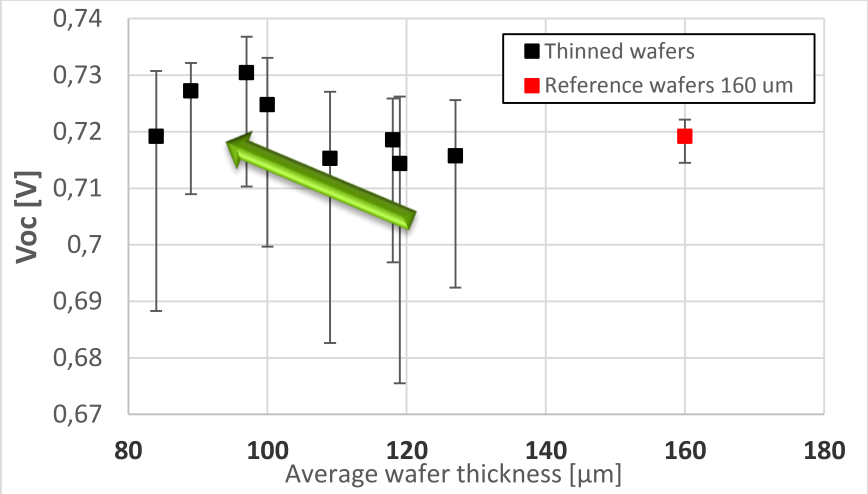
Front side process OK !

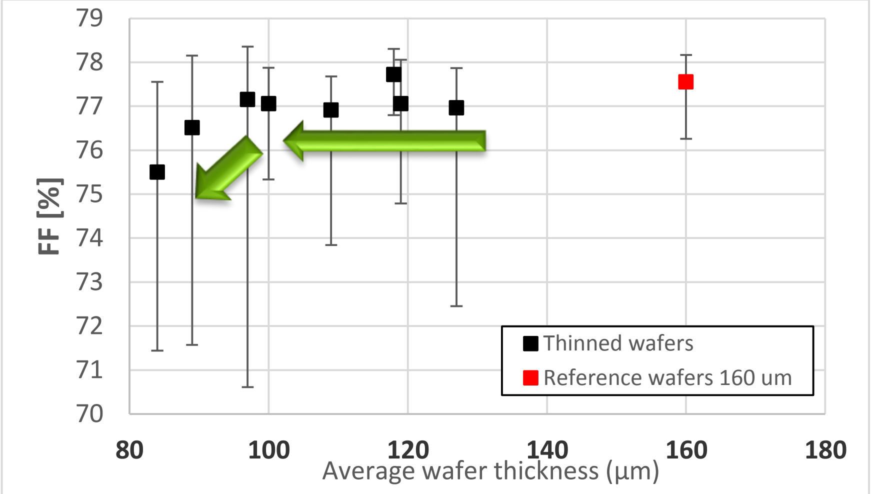
Back side process ongoing
For first Het cells

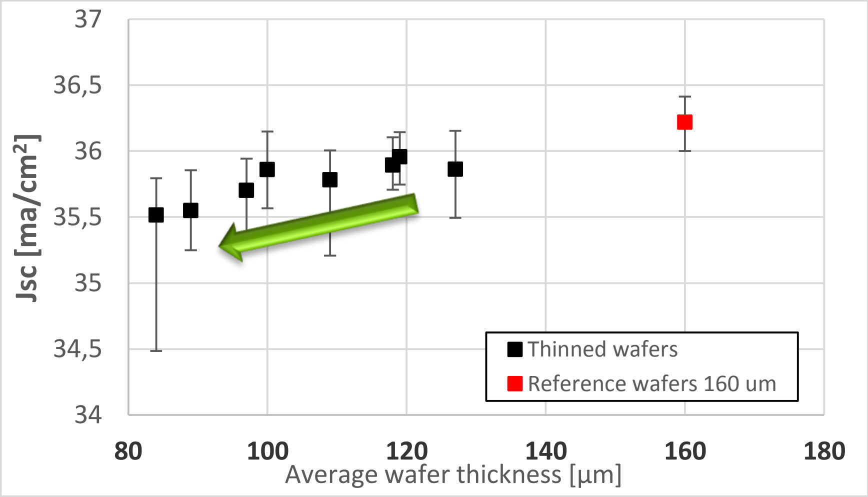
Current results on thin wafers

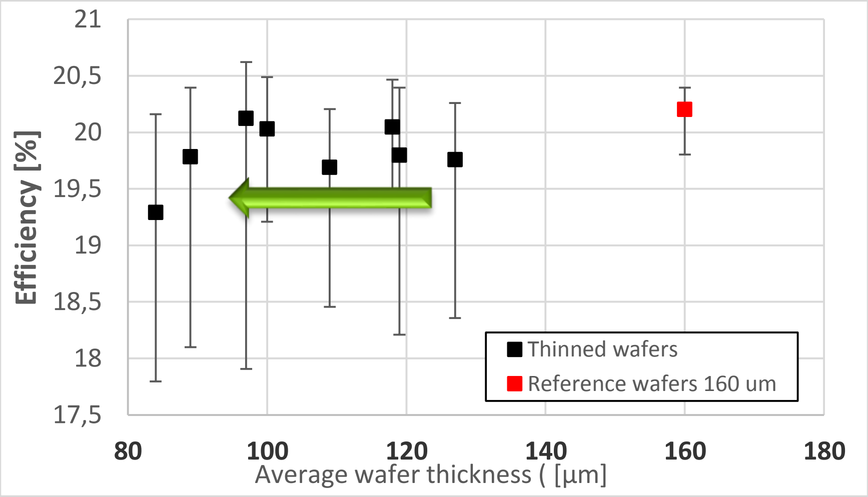


- Thin HET cells (rear emitter) with thicknesses ranging from 84 to 127 µm (INES wafers)
- Industrially compatible (fully automatized) process on INES pilot line / 56-100 cells per batch

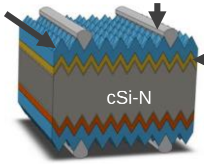






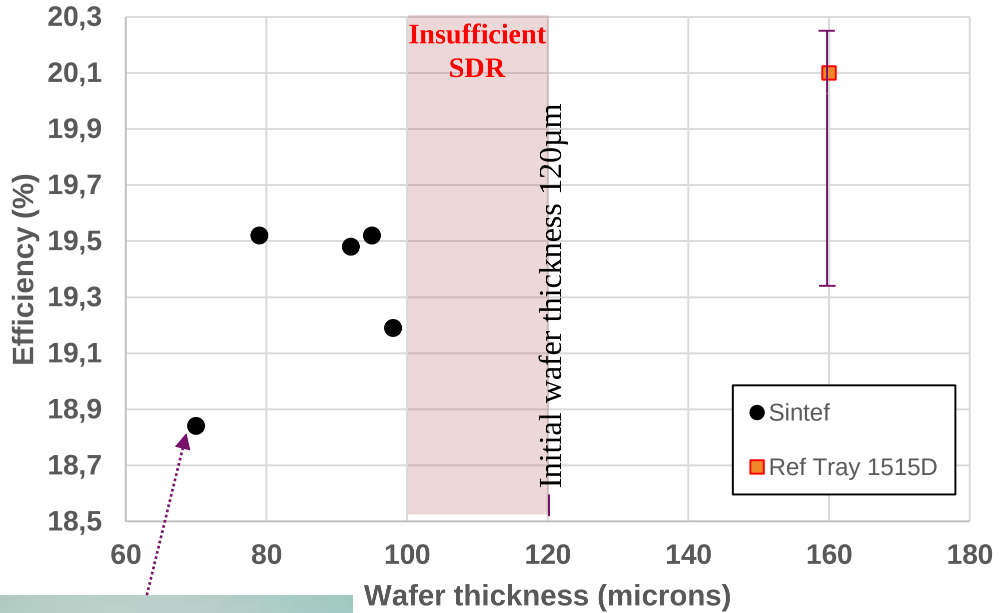


Current results on SINTEF Wafers



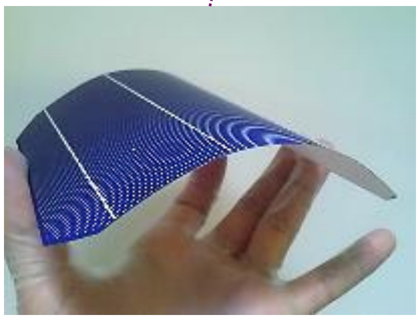
Thin heterojunction a-SI:H/c-Si bifacial solar cells on wafers< 80 µm from 120 µm Sintef wafers

- Integration in our pilot line (automatic handling)



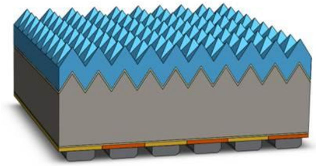
→ Record cell at 19,5% / 80 µm

- Breakage rate: 2 broken cells (70 and 80 µm) out of 12 samples



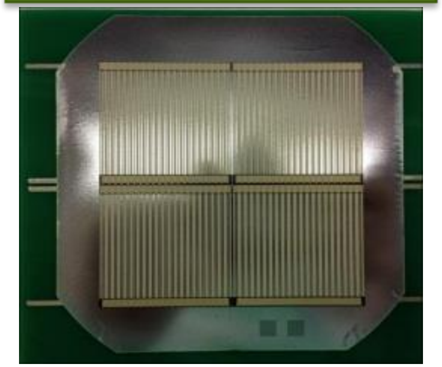
Loss on both Jsc, Voc and FF
Analysis On going

Current results on IBC-HET



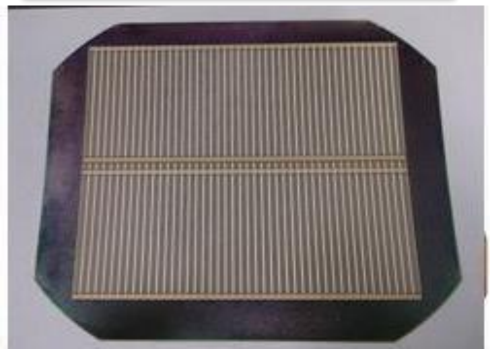
Development of a laser based process for Interdigitated Back Contact (IBC) cells

4 complete cells 5x5 cm

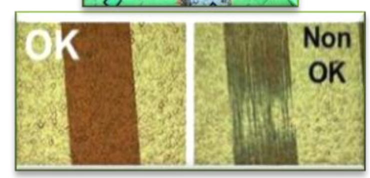


Best cell: 20% Efficiency

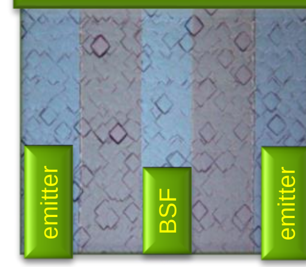
1 complete cell 10x10 cm

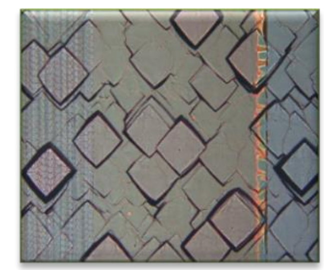


Best cell: 19% Efficiency



Patterning optimised





η≈19%-20%
Moderate Voc ≈ 700mV
Low FF < 70%

Optimisation of laser ablation process.

- ongoing: Scale up and Laser ablation optimization
- Solar cells with optimized patterning coming soon

Upcoming challenges

- Generate std HET solar cells on thin (60-100 µm) wafers using an industrially, fully automatised process for large module (60 cells) fabrication.
- Demonstrate experimentally the novel light trapping structures (honeycomb) designed for ultra-thin 40 µm epifoils
  - KPI 7.1: Increase optical path length to 10 x wafer thickness
- Process the first HET std solar cells on ultra-thin 40 µm epifoils. Develop front side advanced passivation layers.
  - KPI 7.2: Reduction of S_{eff}<5 cm/s on front side textured ultra-thin substrates
- Develop a robust laser based process for high efficiency IBC-HET cell fabrication on thin wafers
- Start a technical economic assessment for std HET and IBC-HET technologies on thin and ultra-thin wafers
  - KPI 7.3: Potential cost reduction evaluation

Module development for ultrathin x-Si cells

Paul Sommeling, ECN

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Objectives

- Main aim for the x-Si part: demonstrate the feasibility of module processing (industrial) based on thin cells
- Cell to module efficiency loss < 1%
- Cost reduction of around 20% compared to current module technology: < 0.5 euro/Wp
- 20 % less material use compared to state of art module (results in more favourable energy payback time and carbon foot print)

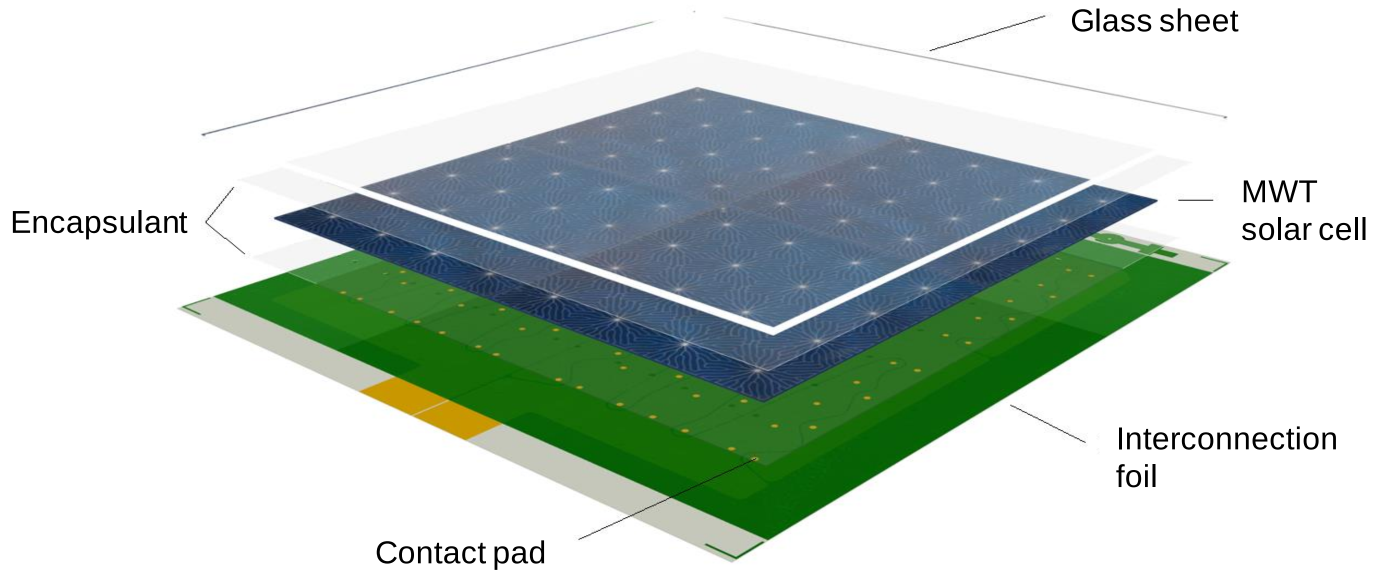
For thin film technologies:

- Interconnection schemes for new device architectures and design of thin film solar cells
- New and simple encapsulation methods for state of the art thin film devices. The aim is high stability at cost reduction for the encapsulation by 20%

Objectives

- In view of fragile thin wafers and cells, back contact module integration has been appointed as the technology of choice in this project. IBC is the preferred cell type

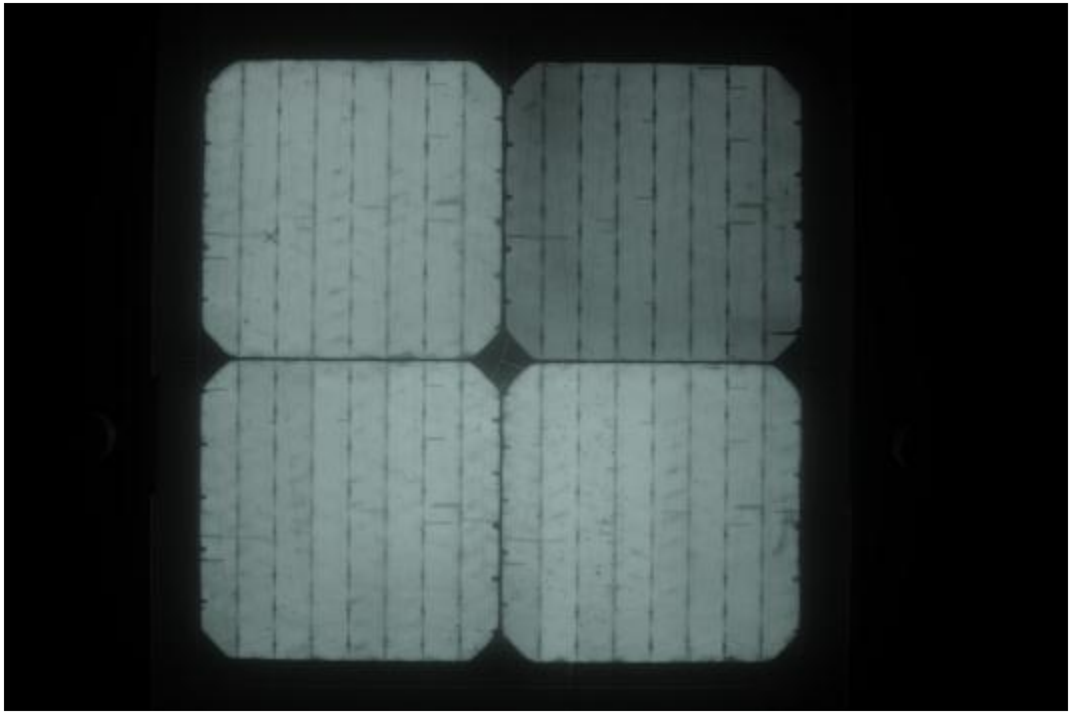
- Advantages: low stress interconnection, no soldering, handling of cells is minimized



Current results

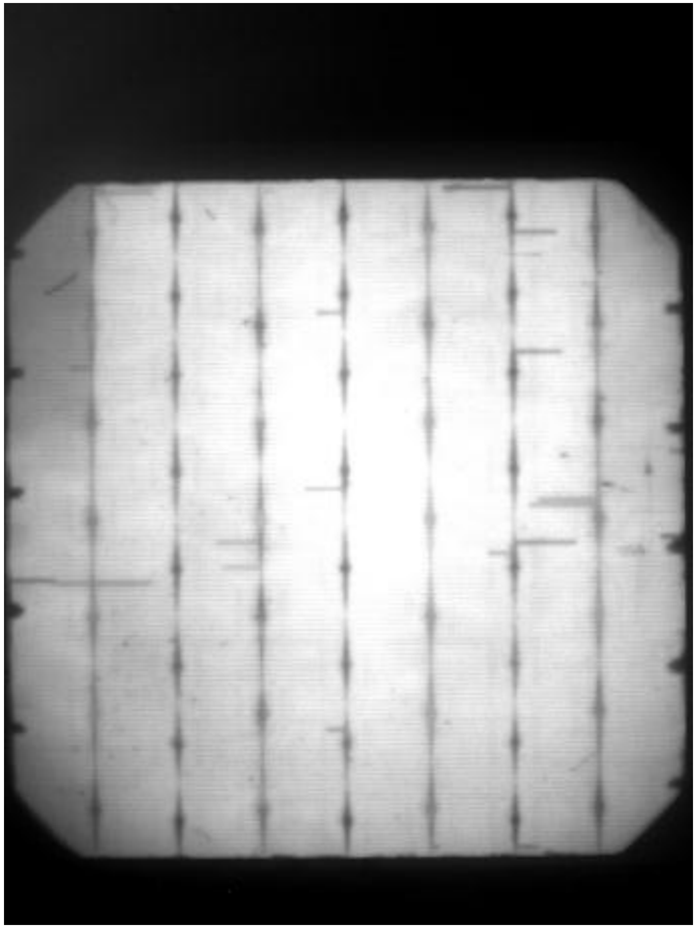
- Successful integration of thin IBC and standard HIT cells (120 µm) in small modules (1cell laminates and 2x2 cells), no cell breakage

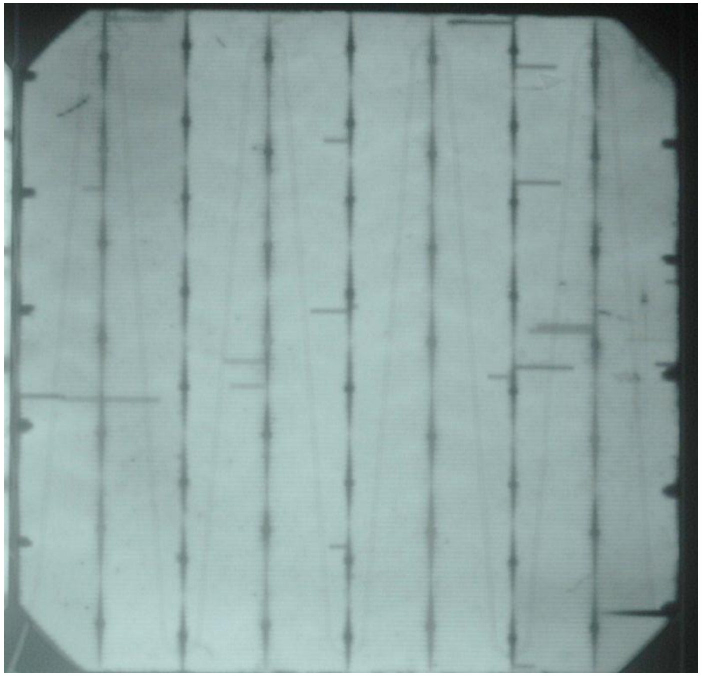
- Thermal cycling test so far: 100 cycles -40°/85°C without problems



EL image: 1 thin cell in a 4 cell mini module

Current results



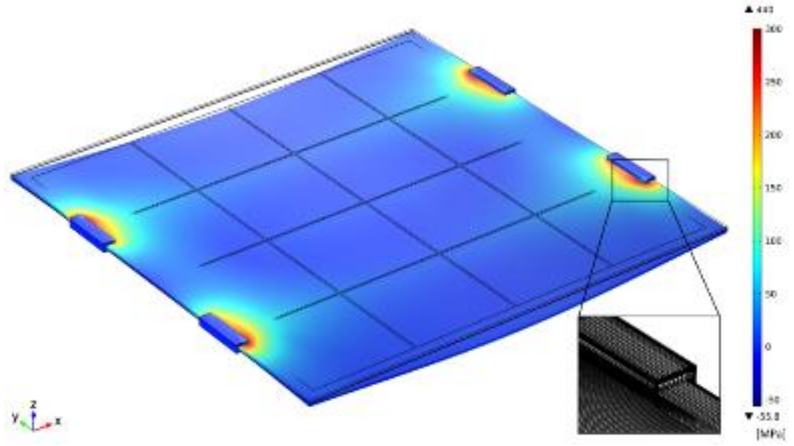


EL images of 120 µm cell before and after module integration

Current results

- First version of a 3D thermomechanical simulation model has been set up by Fraunhofer ISE

- Supports selection of materials combinations in module to minimize cell breakage



Simulated deflection of module under mechanical loading

Upcoming challenges

- Module integration for cells of decreased thickness (stepwise from 120 to 100 and 80 µm respectively)
- Decrease module materials costs (e.g. exchange copper by aluminum in back sheet)
- Produce a few full size modules based on thin IBC cells (80-100 µm, < 1 % cell to module efficiency loss)